A Zvzcs Full Bridge Converter With High Voltage Gain By Solar Energy Source

Nimmy Berchmans, V. Geetha

Abstract: This paper proposes a ZVZCS asymmetrical full-bridge converter with high-voltage gain by different loads. The proposed converter features high-voltage gain, fixed switching frequency and clamped voltages across power switches and output diodes. The control of the converter is implemented with the asymmetrical pulse width modulation technique. The converter achieves zero-voltages witching (ZVS) of all power switches and Zero-current switching (ZCS) of output diodes. The energy shortage and the atmosphere pollution have led to more researches in renewable sources of energy. In this paper, PV module is modelled using Matlab/Simulink. The modeled PV cell act as the dc input source for the converter. The computer simulation of the converter is done using MATLAB/SIMULINK and is interfaced with the mathematical model of PV cell and various waveforms are presented in the paper.

Index Terms: DC–DC converter, high-voltage gain, zero-voltage switching (ZVS), zero-current switching (ZCS), PV module.

1) INTRODUCTION

Recently, the demand for dc/dc converters with high voltage gain has increased because they are required as an interface system between the low voltage sources and the high voltage load which requires higher voltage. This high voltage gain dc to dc converter find applications in electric vehicles, uninterruptible power supplies, fuel cells, and photovoltaic systems [1]–[6]. A conventional boost converter is often used in step-up applications due to its simple structure and low cost. However, it is not suitable for high step-up applications. This is because the conventional boost converter requires an extreme duty cycle to obtain high-voltage gain and its voltage gain is limited due to its parasitic components [11]. The reverse-recovery problem of the output diodes is another important factor in dc/dc converters with high voltage gain. In order to remedy these problems, high step-up dc–dc converters using coupled inductors have been suggested in [9] and [10]. However, they have parasitic oscillations across the switches and diodes. The current-fed converters are often used in high step-up applications due to their inherent low input current ripple characteristic and high-voltage gain [8], [12] but here the voltage stresses of the switches are serious. In order to clamp the voltages across the switches and provide zero-voltage switching (ZVS) features, active snubbers are often employed. The snubbers require additional switches and cause additional conduction losses. As a result, the system efficiency decreases. To remedy these problems, many topologies have been proposed that is the voltage-fed converters such as phase-shift full-bridge (PSFB) converters, which are widely used, show low-voltage stress of the switching devices.

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However, they have some drawbacks including large conduction loss due to circulating current, duty cycle loss, and the voltage spikes across output rectifier. In some of them, auxiliary snubber circuits are employed to suppress the voltage spikes at the secondary side. However, the complexity and the overall cost are increased while the system efficiency decreases due to the additional circuits. In order to overcome these problems, an asymmetrical full bridge converter with high-voltage gain is proposed and shown in Fig. 1. The APWM technique is applied to converter to eliminate switching losses and maintain low conduction loss. The limitation of the maximum duty cycle disappears in this topology. The converter features high-voltage gain, fixed switching frequency, soft-switching operations of all power switches and output diodes, and clamped voltages across power switches and output diodes. The reverse recovery problem of the output diodes is significantly alleviated due to an additional inductor at the secondary side. Therefore, this converter shows high efficiency and it is suitable for high-voltage applications. The dc to dc converters are required as an interface system between photovoltaic systems, fuel cells, and electric vehicles. Increasing population growth and economic development are accelerating the rate at which energy and in particular electrical energy is being demanded. In this highly energy concerned world, focus has been shifted to utilize renewable sources of energy. This has motivated to interface the asymmetrical full bridge converter with a low voltage source and this has resulted in focusing to solar energy. In this paper a zvzcs asymmetrical full bridge converter with high voltage gain interfaced with solar energy and also this circuit is implemented with different types of loads. All methods of electricity generation have consequences for the environment, so meeting this growth in demand, while safe- guarding the environment poses a growing challenge. Renewable energy technology offers the promise of clean, abundant energy gathered from self-renewing resources such as sun, wind, water, earth and plant. Renewable energy technology offer important benefits compared to those of conventional energy sources. These types of systems, which are not connected to the main utility grid, are also used in stand-alone applications and operate independently and reliably. The best applications for these systems are in remote places, such as rural villages, in telecommunications, etc.

2)ANALYSIS OF ZVZCS FULL-BRIDGE CONVERTER WITH HIGH VOLTAGE GAIN

The circuit diagram of the converter with high-voltage gain is shown in fig 1. The converter has four power switches S1 through S4. There is a clamping capacitor Cc between top side switches S1 and S3 of two switch bridges [21]. The voltages across the switches S1 and S2 in the first bridge are confined to the input voltage Vin. The clamping capacitor Cc can clamp the voltages across the switches S3 and S4 in the second bridge. The output stage of the converter has a voltage doubler structure that consists of the secondary winding N2 of the transformer T, the serial inductor Ls, the output capacitors Co1, and Co2, and the output diodes Do1 and Do2.In the voltage doubler structure, the voltage gain increases and the voltage stresses of the output diodes are confined to the output voltage Vo without any auxiliary circuits.

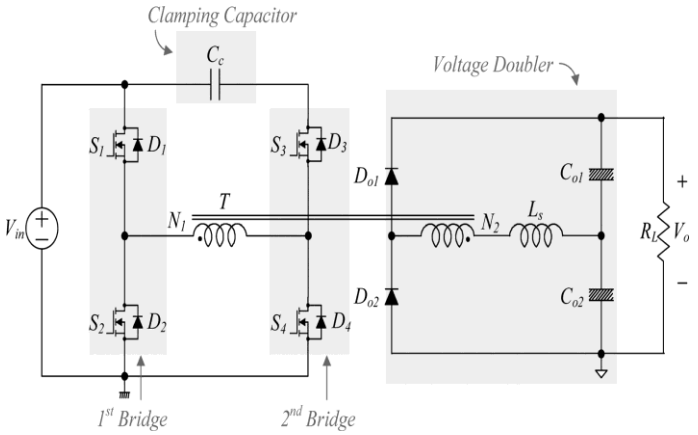

Fig -1: Circuit diagram

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Fig. 2 shows the equivalent circuit of the converter. The diodes D1 through D4 are the intrinsic body diodes of all switches. The capacitors C1 through C4 represent their parasitic output capacitances. The transformer T is modeled as the magnetizing inductance Lm and the ideal transformer that has a turn ratio of 1: n (n = N2 /N1). Its leakage inductance is included in the serial inductor Ls.

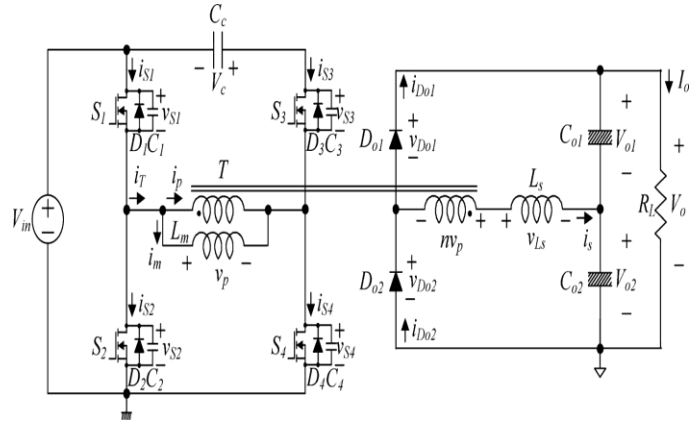

Fig- 2:-Equivalent circuit of the converter

To simplify the analysis, it is assumed that the clamping capacitor Cc has a large value and the voltage across Cc is constant as VC under a steady state. Similarly, the output capacitor voltages are assumed to be constant as VO 1 and VO 2, respectively. The theoretical waveforms of the proposed converter are shown in Fig. 3. The switch S1 (S4) and the switch S2 (S3) are operated asymmetrically and the duty cycle D is based on the switch S1 (S4). A small delay between driving signals for S1 (S4) and S2 (S3) is a dead time for the switches. It prevents cross conduction and allows ZVS. The converter consist of four modes of operation as shown in Fig. 4.Before t0 , the switches S2 and S3 , and the output diode Do 1 are conducting. At t0, the magnetizing current im and the secondary current is arrive at their minimum values Im2 and −IDo1, respectively.

Mode 1 [t0, t1]: At t0, the switches S2 and S3 are turned OFF. Then, the energy stored in the magnetic components starts to charge/discharge the parasitic capacitances C1 through C4 .Therefore, the voltages vS 2 and vS 3 start to rise from zero. Similarly, the voltage vS 4 starts to fall from Vin + Vc and the voltage vS 1 starts to fall from Vin . Since all the parasitic output capacitances C1 through C4 are very small, this transition time interval is very short and it is ignored in Fig. 3. When the voltages vs 1 and vs 4 arrive at zero, their body diodes D1 and D4 are turned ON. Then, the gate signals are applied to the switches S1 and S4. Since the currents have already flown through D1 and D4 and the voltages vs1 and vs 4 are clamped as zero before the switches S1 and S4 are turned ON, zero-voltage turn-ON of S1 and S4 is achieved. With the turn-ON of S1 and S4, the primary voltage VP across Lm is Vin.

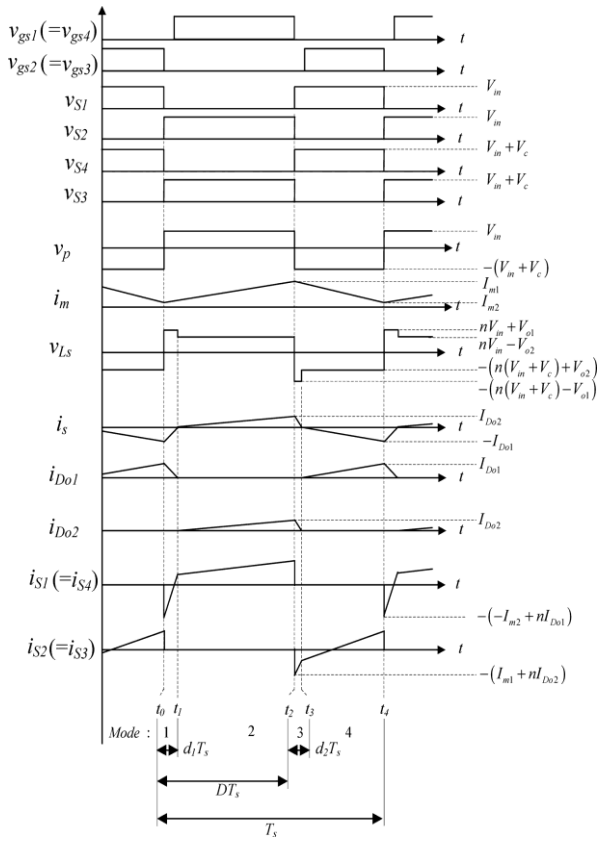

Fig. 3:- Theoretical waveforms

Mode 2 [t1, t2]: At t1, the currents is and iDo1 arrive at zero and the diode Do 1 is turned OFF. Then, the output diode Do 2 is turned ON and its current increases linearly. Since the current changing rate of Do 1 is controlled by the serial inductor Ls, so its reverse-recovery problem is significantly alleviated. At the end of this mode, the currents im and is arrive at their maximum values Im1 and IDo2, respectively.

Mode 3 [t2, t3]: Similar to mode 1, the switches S1 and S4 are turned OFF at t2. The parasitic capacitors C1 and C4 start to be charged from zero, whereas the parasitic capacitors C2 and C3 start to be discharged from Vin and Vin + Vc, respectively. The transition time interval is very short and it is ignored. After the parasitic capacitors are fully charged and discharged, the voltages vS 2 and vS 3 become zero and the body diodes D2 and D3 are turned ON. Then, the gate signals are applied to the switches S2 and S3. Since the currents have already flown through D2 and D3 and the voltages vS 2 and vS 3 are clamped as zero, zero-voltage turn-ON of S2 and S3 is achieved. With the turn-ON of S2 and S3, the voltage vp across Lm is − (Vin+Vc).

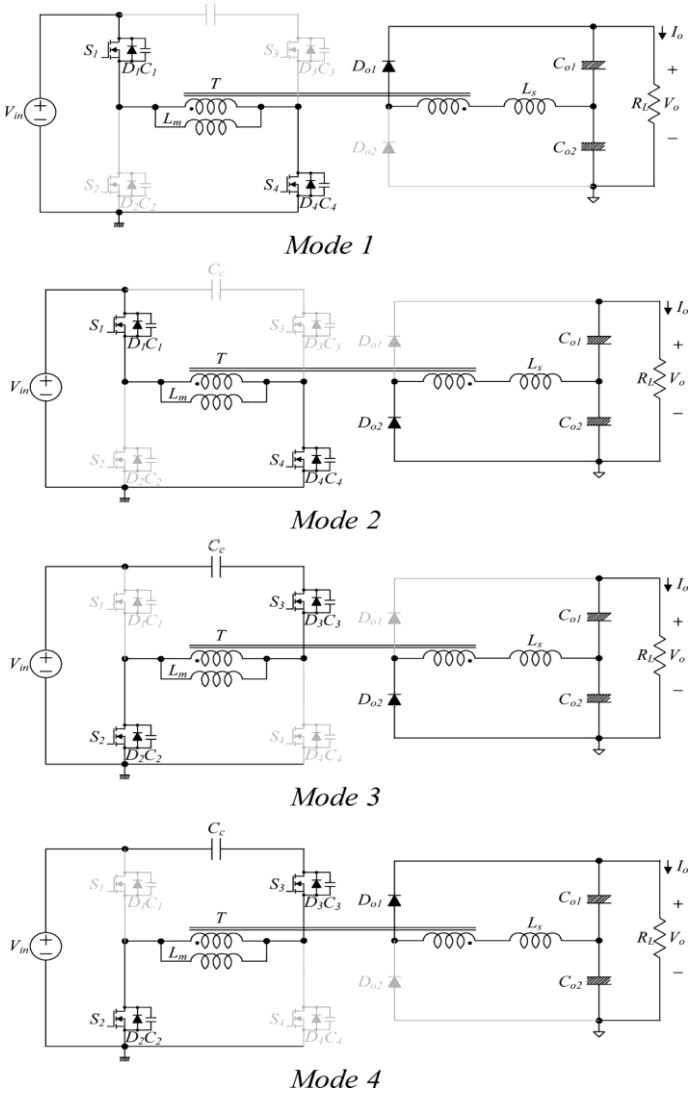

Fig. 4:- Operating Modes.

Mode 4 [t3, t4]: Similar to mode 2, the currents is and iDo2 arrive at zero and the diode Do 2 is turned OFF at t3. Then, the output diode Do 1 is turned ON and its current increases linearly. Since the current changing rate of Do 2 is controlled by Ls, its reverse-recovery problem is significantly alleviated. At the end of this mode, the currents im and is arrive at Im2 and −IDo1, respectively.

Clamping capacitor voltage Vc is

Vc = (2D-1/1-DVin (1)

Where D-duty cycle, Vin-input voltage.

Voltage gain M=V0/Vin

=n (1-2k) D/ (D+ (1-2D)k)(1-D-(1-2D)k) (2)

d1=kD (3)

d2=k(1-D) (4)

Switching period Ts=1/f (5)

ZVS Conditions for the Switches S1 through S4:-

From Fig. 3, there is no current cancellation between ip (=nis) and im at t2. Therefore, for ZVS of S2 and S3, the total energy stored in Lm and Ls should be larger than the energy stored in C1 through C4. Namely, the following condition should be satisfied:

$$\frac{L_m I_{m1}^2}{2} + \frac{L_s I_{Do2}^2}{2} > \frac{(C1+C2)\,V_{in}^2}{2} + \frac{(C3+C4)\,(V_{in}+V_c)^2}{2} \quad (6)$$

Since n, Im1, and IDo1 always have positive values and C1 through C4 are quite small, it can be easily seen that the inequality of (6) is satisfied. On the other hand, there is current cancellation between ip (= nis) and im at t0. Therefore, for ZVS of S1 and S4, the energy difference between the energies stored in Lm and Ls should be larger than the energy stored in C1 through C4 as follows:

$$-\frac{L_m I_{m2}^2}{2} + \frac{L_s I_{Do1}^2}{2} > \frac{(C1+C2)\,V_{in}2}{2} + \frac{(C3+C4)\,(V_{in}+V_c)^2}{2} \quad (7)$$

This condition can be used to determine Lm.

3) MATHEMATICAL MODEL FOR A PHOTOVOLTAIC MODULE

Regardless of the intermittency of sunlight, solar energy is widely available and is free. It can generate direct current electricity without environmental impact and contamination when exposed to solar radiation. Being a semiconductor device, the PV system is static, quiet, free of moving parts, and has little operation and maintenance costs. The output characteristics of a PV module depend on the solar insolation, the cell temperature and the output voltage of the PV module. In this paper, a step-by-step procedure for simulating PV module with subsystem blocks, with user-friendly icons and dialog in the same way as Matlab/ Simulink block libraries is developed. The photovoltaic panel can be modeled mathematically as given in equations (8)- (11) [18] – [20].

Module photo-current:

Iph =[Iscr+Ki (T-298]*λ/1000 (8)

Module reverse saturation current:

Irs=Iscr/ [exp (qVoc/NskAT)-1] (9)

The module saturation current I0 varies with the cell temperature, which is given by

$Io=Irs[T/Tr]^3$ exp[q*Ego/Bk{(1/Tr)-(1/T)}] (10)

The current output of PV module is
Ipv=Np*Iph-Np*Io[exp{q*(Vpv+IpvRs)/NsAkT}-1 (11)

Where Vpv = Voc, Np = 2 and Ns = 72

First step is to convert the module operating temperature given in degrees Celsius to Kelvin shown in Fig:-5

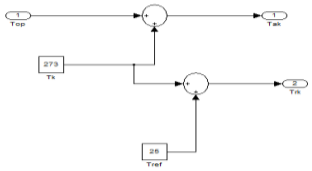

Fig 5:- Circuit under subsystem 1

Then find module photo current, module reverse saturation current Irs, module saturation current Io and finally current output of PV module Ipv. The final model is shown in Figure 6. The workspace is added to measure Ipv, Vpv, Ppv in this model.

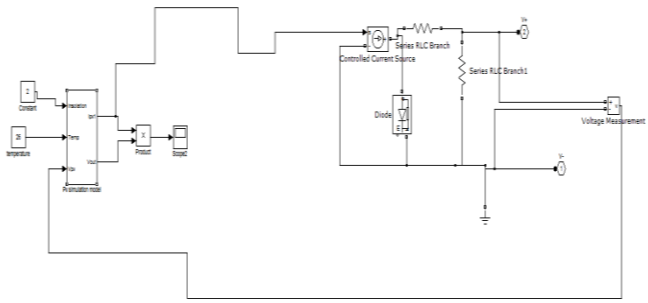

Fig 6:- Simulink model of PV module

The final model takes irradiation, operating temperature in Celsius and module voltage as input and gives the output current Ipv and output voltage Vpv. In the paper, the PV module is modelled using the above eqns and interfaced with asymmetrical full bridge converter ie, solar panel is made as the dc source of the converter.

4) SIMULATION AND RESULTS

The converter of Fig.1 with solar energy source is simulated using MATLAB/SIMULINK for the following input and output data specifications.

- **a)** Input voltage, Vin: 48V
- **b)** Output voltage, Vo: 368V
- **c)** full-load power, Pout: 150
- **d)** Switching frequency ,fs : 74 kHz.

As per the analysis, the voltage gain is 8 and turns ratio of 3 and Ls (90μH) and Lm (132μH). The simulated circuit diagram of the converter with R, RL, RLE loads by PV module as its source are shown in fig 7, 9&11. The output voltages are shown in fig 8, 10, 12.

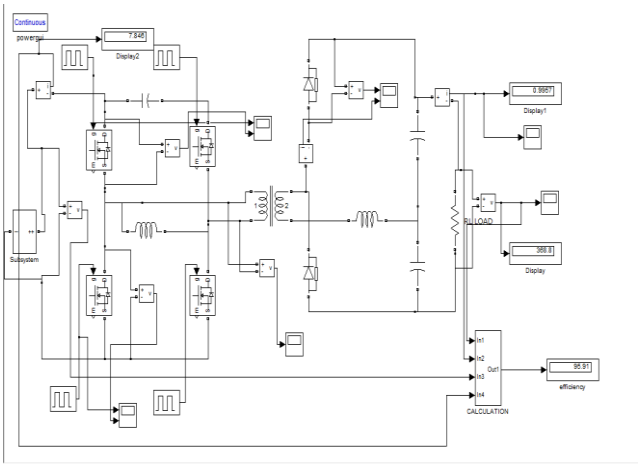

Fig-7:- Simulated circuit diagram of zvzcs asymmetrical full bridge converter with solar energy as dc source

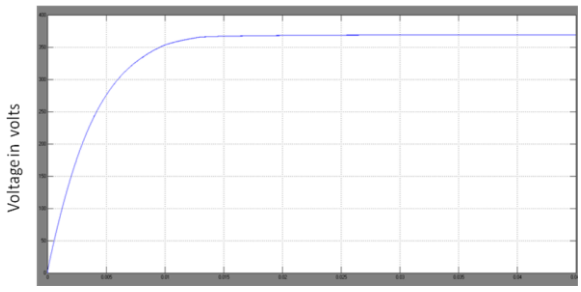

Fig-8:- Output voltage waveform for R load

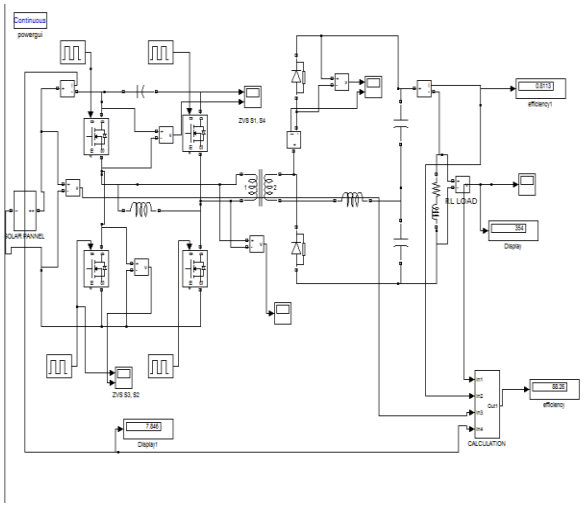

Fig-9:-Simulated circuit diagram of converter with RL load.

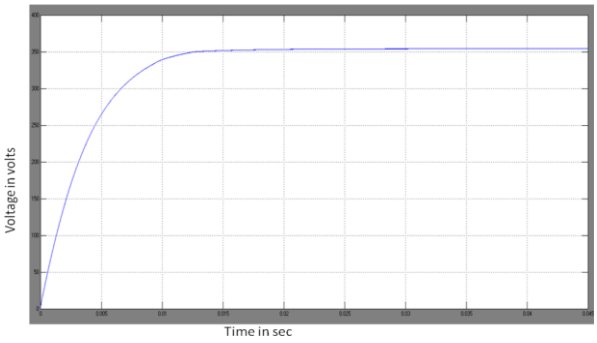

Fig-10:- Output voltage waveform for RL load

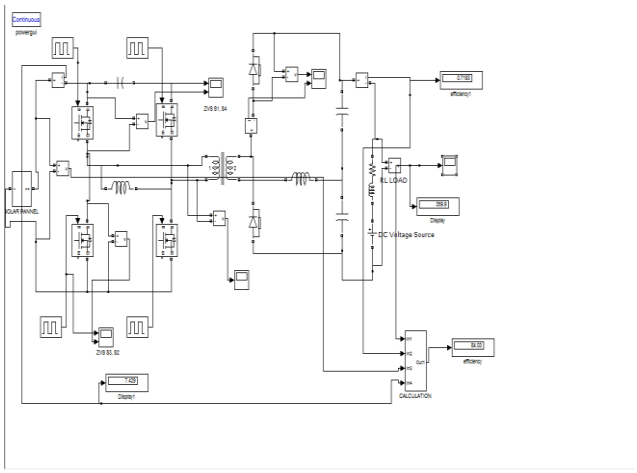

Fig-11:-Simulated circuit diagram of converter with RLE load.

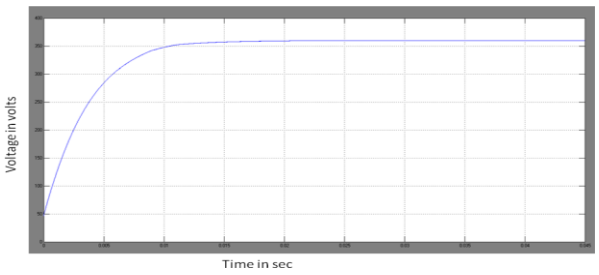

Fig-12:- Output voltage waveform for RLE load

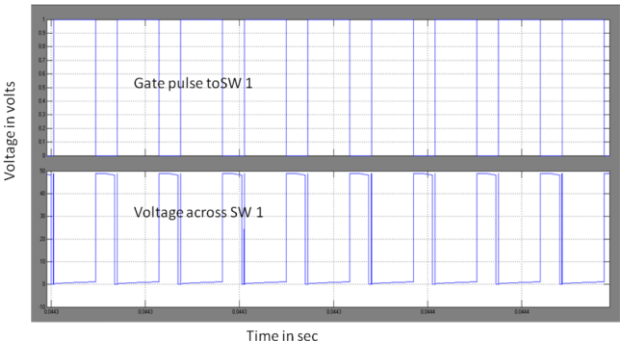

Fig-13:- Waveforms are showing gate pulse to switch S1, voltage across switch S1.

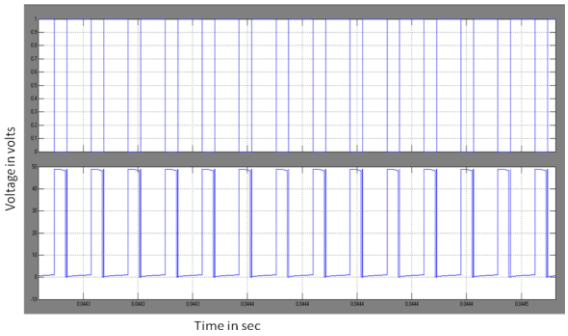

Fig-14:- Waveforms are showing gate pulse to switch S2, voltage across switch S2.

Fig. 13 and 14 shows the ZVS operations of the power switches. The voltages across the switches go to zero before the gate pulses are applied to the switches. Since the switch voltages are clamped as zero before the gate pulses are applied, the ZVS turn-ON of the switches is achieved.

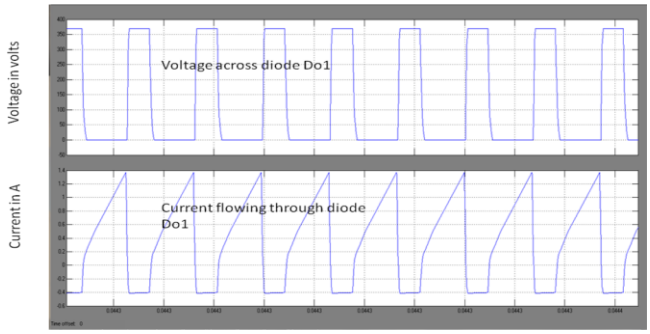

Fig-15:- Waveforms showing voltage across and current flowing through, diode D01.

Fig. 15 shows ZCS of the output diodes. After the diode currents fall to zero, the voltages across the diode rise to the output voltage Vo. Therefore, the ZCS turn-OFF of the output diodes is achieved.

LOAD	VOLTAGE	EFFICIENCY	ZVS	ZCS
R LOAD	368.8V	95.91%	Achieved	Achieved
RL LOAD	354V	88.26%	Achieved	Achieved
RLE LOAD	356V	84.03%	Achieved	Achieved

Fig 16:-Comparison table

Fig16 shows the comparison table of different loads. Here R load has the highest efficiency and for all loads(R, RL, RLE)-ZVS and ZCS are achieved.

5. CONCLUSION

In this paper, the zvzcs asymmetrical full bridge converter with high voltage gain is interfaced with a PV module. The converter is able to provide a high efficiency and high-voltage gain with relatively low transformer turns ratio. The ZVS of all power switches and ZCS of the output diodes are achieved. Therefore, the converter is suitable for high-voltage applications. In this paper, both dc and solar energy sources are used as input source. And from both the result high voltage gain and high efficiency is obtained. So in this highly energy concerned world effective utilization of solar energy with this concept of converter can be used for many applications. Also from this paper performance of different types of loads are studied and from that we obtained the conclusion that R load has the highest efficiency and for all loads(R, RL, RLE)-ZVS and ZCS are achieved.

6. REFERENCES

[1]. R. J. Wai, W. H. Wang, and C. Y. Lin, “High-performance stand-alone photovoltaic generation system,” IEEE Trans. Ind. Electron., vol. 55, no. 1, pp. 240–250, Jan. 2008.

[2]. C. Wang and M. H. Nehrir, “Power management of a standalone wind/photovoltaic/fuel cell energy system,” IEEE Trans. Energy Convers., vol. 23, no. 3, pp. 957–967, Sep. 2008.

[3]. R. J. Wai and W. H. Wang, “Grid-connected photovoltaic generation system,” IEEETrans. CircuitsSyst. I, Reg. Papers, vol. 55, no. 3, pp. 953–964, Apr. 2008.

[4]. M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Fules, “Voltage multiplier cells applied to non-isolated DC-DC converters,” IEEE Trans. Power Electron., vol. 23, no. 2, pp. 871–887, Mar. 2008.

[5]. E. H. Ismail, M. A. Al-Saffar, A. J. Sabzali, and A. A. Fardoun, “A family of single-switch PWM converters with high step-up conversion ratio,” IEEE Trans. Circuit Syst. I, vol. 55, no. 4, pp. 1159–1171, May 2008.

[6]. W.-S. Liu, J.-F. Chen, T.-J. Liang, and R.-L. Lin, “Multicascoded sources for a high-efficiency fuel-cell hybrid power system in high-voltage. application,” IEEE Trans. Power Electron., vol. 26, no. 3, pp. 931–942, Mar.

[7]. Z. Liang, R. Guo, J. Li, and A. Q. Huang, “A high-efficiency PV modal integrated DC/DC converter for PV energy harvest in FREEDM systems,” IEEE Trans. Power Electron., vol. 26, no. 3, pp. 897–909, Mar. 2011

[8]. L. Zhu, K. Wang, F. C. Lee, and J. S. Lai, “New start-up schemes for isolated full-bridge boost converters,” IEEE Trans. Power Electron., vol. 18, no. 4, pp. 946–951, Jul. 2003

[9]. Q. Zhao, F. Tao, Y. Hu, and F. C. Lee, “Active-clamp DC/DC converter using magnetic switches,” in Proc. IEEE Appl. Power Electron. Conf.Expo., 2001, pp. 946–952.

[10]. D. A. Grant, Y. Darroman, and J. Suter, “Synthesis of tapped-inductor switched-mode converters,” IEEE Trans. Power Electron., vol. 22, no. 5, pp. 1964–1969, Sep. 2007.

[11]. L.-S. Yang, T.-J. Liang, and J.-F. Chen, “Transformerless DC-DC converters with high step-up voltage gain,” IEEE Trans. Ind. Electron., vol. 56, no. 8, pp. 3144–3152, Aug. 2009

[12]. E. Adib and H. Farzanehfard, “Zero-voltage transition current-fed full bridge PWM converter,” IEEE Trans. Power Electron., vol. 24, no. 4, pp. 1041–1047, Apr. 2009.

[13]. Y. Jang and M. M. Jovanovic, “A new family of full-bridge ZVS converters,” IEEE Trans. Power Electron., vol. 19, no. 3, pp. 701–708, May 2004.

[14]. M. Borage, S. Tiwari, S. Bhardwaj, and S. Kotaiah, “A full-bridge DC-DC converter with zero-voltage-switching over the entire conversion range,” IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1743–1750, Jul. 2008.

[15]. Y. Jang and M. M. Jovanovic, “A new PWM ZVS full-bridge ZVS converter,” IEEE Trans. Power Electron., vol. 22, no. 3, pp. 987–994, May 2007.

[16]. A. Fiedler and H. Grotstollen, “Investigation of asymmetrical phase shifted full bridge,” in Proc. IEEE IECON, 1995, pp. 434–439.

[17]. A. J. Zhang, G. Huang, and Y. Gu, “Asymmetrical full bridge DC-to-DC converter,” U.S. Patent 6 466 458, Oct. 15, 2002

[18]. S.Chowdhury, S.P.Chowdhury, G.A.Taylor, and Y.H.Song,“Mathematical Modeling and Performance Evaluation of a Stand-Alone Polycrystalline PV Plant with MPPT Facility,” IEEE Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century, July 20-24, 2008, Pittsburg, USA.

[19]. Jee-Hoon Jung, and S. Ahmed, “Model Construction of Single Crystalline Photovoltaic Panels for Real-time Simulation,” IEEE Energy Conversion Congress & Expo, September 12-16, 2010, Atlanta, USA.

[20]. S. Nema, R.K.Nema, and G.Agnihotri, “Matlab / simulink based study of photovoltaic cells / modules / array and their experimental verification,” International Journal of Energy and Environment, pp.487-500.500, Volume 1, Issue 3, 2010.

[21]. Hyun-Lark Do, “Asymmetrical Full-bridge Converter with High-Voltage Gain” IEEE Trans. Power Electron, vol. 27, no. 2, February 2012.