Digital Control Of A Buck Converter Using An 8 Bit STM Microcontroller

Muhammad Umar Abbasi

Abstract: The aim of this paper is to describe the modeling and digital control of a buck converter using an 8 bit STM microcontroller. The modeling procedure including the inductor dc resistance and capacitor esr using both the circuit averaging as well as the state space averaging method is described in a simple manner. The resulting small signal control to output transfer function is used to select a suitable PID controller in order to obtain satisfactory control loop performance and also maintain ease of implementation. Practical issues involved in implementing digital control using 8 bit microcontrollers are discussed. MATLB Simulations and practical implementation results on a STM8S controller are presented to validate the modeling and controller design approach. The perspective applications of this controller are discussed.

Index Terms: buck convertor; average circuit modeling; state space modeling; digital control; 8 bit STM controller; PID Controller; MATLAB

1 INTRODUCTION

The aim of this paper is to describe the sampled data modeling of a switching regulator and the practical implementation of a digital compensator on an 8 bit microcontroller. The major blocks comprising a digital control loop are described and their transfer functions are derived. Practical issues involved in digital control using low cost 8 bit microcontrollers are discussed and results are presented. Modeling of switching regulators in continuous time domain is a well established discipline. Introduced by S. Cuk [1], the averaging approach for switching regulator modeling is a well known and widely popular technique. In this approach, the non-linear switching waveforms are averaged over one switching period thereby removing switching ripple and associated non-linearity. This is justified as in a well designed converter the switching ripple is small as compared to dc quantities. Small signal models can then be derived and used for control system design. The advantages of this approach are its simplicity and ease of use. Moreover, analog control design tools can be used for designing control systems. However, these models are accurate up to half of the switching frequency. Discreet time modeling of switching regulators was introduced by J. Packard [2]. In this approach, instead of averaging, converter waveforms are described at the instant of sampling [9]. This captures the behavior of converter at the sampling instant which is then extended over entire switching period. This modeling results in exact small signal models of switching regulators which can be used to design control systems using MATLAB. These models are accurate throughout the frequency range. However such models suffer from the complexity of the results as well as lack of close form results. Sampled data modeling approach introduced by A.R. Brown [3] combines the simplicity of average modeling approach with the accuracy of discreet time modeling technique. The entire system is modeled in continuous domain using conventional Laplace transform transfer functions. The delay associated with the digital control loops is modeling using a single delay block.

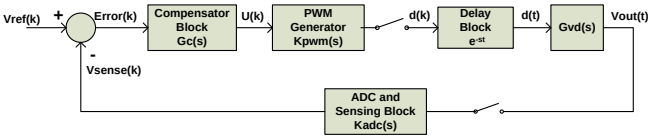

Fig. 1. *Sampled Data Model*

This retains the closed form results nature of the model and also incorporates the physical delays associated with the practical systems. In this work, a sampled data model of a buck converter is used to model the system and select compensator. The efficacy of the compensator designed is validated through MATLAB simulations. The digital loop is closed around an 8 bit microcontroller from ST Micro. The aim of this work is to provide an easy to understand derivation of sampled data model as well as demonstrate the capability of an 8 bit system to control a switching converter with acceptable performance for a given application. The paper is presented in following way: section 2 and 3 provide derivation of average circuit modeling approach and state space averaging approach for a special case of buck converter including inductor dc resistance and capacitor esr. It is assumed that the converter operates in continuous conduction mode. Section 4 provides description of transfer functions for various building blocks of a digital control loop. Section 5 provides simulation results of compensator designed in MATLAB as well as practical implementation details. Section 6 describes potential applications of this converter.

2. Average Circuit Modeling

We begin with the basic buck converter schematic as shown below. Note that inductor dc resistance and capacitor esr are ignored initially and will be incorporated later.

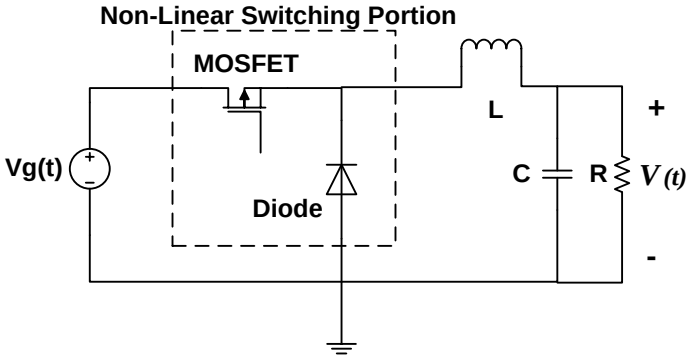

Fig. 2. *Buck Converter*

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The aim of the modeling is to replace the non linear switching part of the converter with linear circuit elements so that the circuit can be solved for transfer functions using linear circuit analysis tools. The buck converter in continuous conduction mode operates periodically in two states; subinterval one in which MOSFET switch is ON and diode is off; subinterval two in which MOSFET switch is OFF and diode is ON. In first step, both these subintervals along with the equations describing inductor current and output voltage are shown:

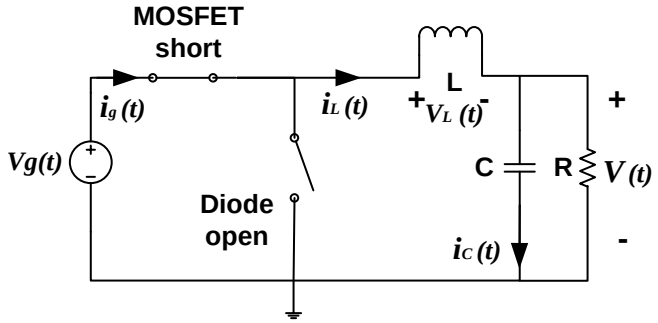

Fig. 3. *Sub Interval One*

$$0 \le t \le d(t)*Ts \tag{1}$$

$$V_L(t) = L\frac{di_L(t)}{dt} = V_g(t) - V(t) \tag{2}$$

$$i_C(t) = C\frac{dV(t)}{dt} = i_L(t) - \frac{V(t)}{R} \tag{3}$$

$$i_g(t) = i_L(t) \tag{4}$$

Where d(t) is the duty ratio function representing the time MOSFET switch is ON. Ts is the switching period. Equation (1) represent the time duration when MOSFET is ON.

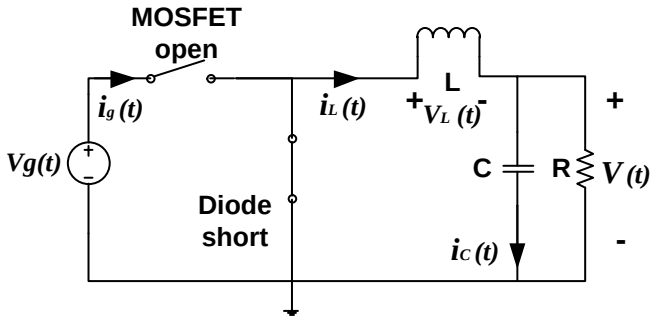

Fig. 4. *Sub Interval Two*

$$d(t)*Ts \le t \le Ts \tag{5}$$

$$V_L(t) = L\frac{di_L(t)}{dt} = -V(t) \tag{6}$$

$$i_C(t) = C\frac{dV(t)}{dt} = i_L(t) - \frac{V(t)}{R} \tag{7}$$

$$i_g(t) = 0 \tag{8}$$

Applying the averaging operator $<x(t)>_{Ts}$ [4] to these equations and combining for both intervals using duty cycle functions d(t) and d'(t),where d(t) represents the time of switching period during which MOSFET is ON and d'(t) = 1-d(t), we arrive at large signal model of buck converter:

$$L\frac{d<i_L(t)>_{Ts}}{dt} = [<Vg(t)>_{Ts} - <V(t)>_{Ts}]*d(t) + [-<V(t)>_{Ts}]*d'(t) \tag{9}$$

$$C\frac{d<V(t)>_{Ts}}{dt} = <i_L(t)>_{Ts} - \frac{<V(t)>_{Ts}}{R} \tag{10}$$

$$<i_g(t)>_{Ts} = <i_L(t)>_{Ts} * d(t) \tag{11}$$

The above equations describe the large signal model of the buck converter. In order to derive the small signal model of the buck converter, a steady state solution is assumed to exist (Vg, V, I, D) and following variables are perturbed and linearized:

$$<V_g(t)>_{Ts} = V_g + v_g(t),\ <i_g(t)>_{Ts} = I_g + \hat{i}_g(t),$$
$$<V(t)>_{Ts} = V + \hat{v}(t),\ <i_L(t)>_{Ts} = I + \hat{i}_L(t), \tag{12}$$
$$d(t) = D + \hat{d}(t),\ d'(t) = D - \hat{d}(t)$$

Where the small perturbation in x(t) is denoted as x̂(t) and it is further assumed in accordance with small ripple approximation that: x̂(t) << X i.e. the perturbation is very small as compared to dc quantities. Equations (9), (10) and (11) become:

$$L\frac{d[I + \hat{i}_L(t)]}{dt} = [V_g + v_g(t) - V - \hat{v}(t)]*[D + \hat{d}(t)] + [-V - \hat{v}(t)]*[D - \hat{d}(t)] \tag{13}$$

$$C\frac{d[V + \hat{v}(t)]}{dt} = I + i_L(t) - \frac{V + \hat{v}(t)}{R} \tag{14}$$

$$I_g + i_g(t) = [I + i_L(t)]*[D + d(t)] \tag{15}$$

After ignoring DC and higher order terms, one arrives at the small signal model of buck converter:

$$L\frac{d\hat{i}_L(t)}{dt} = [D*\hat{v}_g(t)] + [V_g*d(t)] - \hat{v}(t) \tag{16}$$

$$C\frac{d\hat{v}(t)}{dt} = \hat{i}_L(t) - \frac{\hat{v}(t)}{R} \tag{17}$$

$$\hat{i}_g(t) = [D*\hat{i}_L(t)] + [d(t)*I] \tag{18}$$

And the equivalent circuit is shown below:

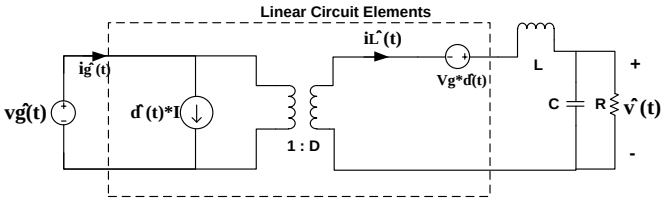

Fig. 5. *Equivalent Average Circuit Model*

This is the same result as obtained in [4]. In order to include the effect of inductor dc resistance and capacitor esr, resistances rl and rc are introduced respectively. The primary

side voltage source vĝ (t) is set to zero so as to assume zero variation in supply voltage. This result in elimination of dc transformer and following circuit is obtained.

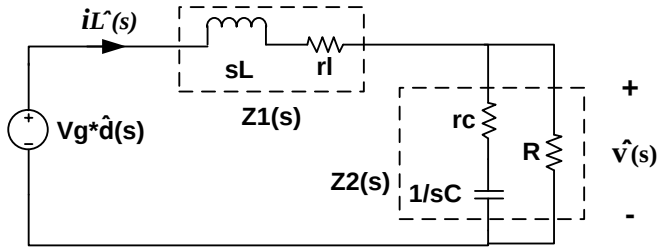

Fig. 6. *Equivalent Impedances*

Here rl and rc represent the dc resistance of inductor and esr of capacitor respectively. Also all the impedances are represented in Laplace domain. This circuit can be very easily simplified to obtain Gvd(s) using voltage divider rule as shown below:

$$G_{vd}(s) = \frac{\hat{v}(s)}{\hat{d}(s)} = \frac{V_g * Z2(s)}{Z1(s) + Z2(s)} \tag{19}$$

$$Z1(s) = rl + sL, \qquad Z2(s) = R \,||\, (rc + \frac{1}{sC}) \tag{20}$$

$$G_{vd}(s) = \frac{Vg * R * (s * C * rc + 1)}{s^2 * L * C * (R + rc) + s * (L + rc * rl * C + R * C * (rc + rl) + R + rl} \tag{21}$$

This is the desired control to output transfer function and coincides with the results such as those given in [7].

3. State Space Average Modeling

The general state space representation of a switching converter is given by following two equations [4]:

$$\frac{d\,x(t)}{d(t)} = A * x(t) + B * u(t) \tag{22}$$

$$y(t) = C * x(t) + E * u(t) \tag{23}$$

Where x(t) is the state vector of the system consisting of inductor current and capacitor voltage and is given by:

$$x(t) = \begin{bmatrix} i_L(t) \\ V_C(t) \end{bmatrix} \tag{24}$$

U(t) is the system input vector which consists of input source Vg(t). We define the state vectors in the following manner [4]:

$$\begin{aligned} A &= D * A1 + D' * A2 \quad B = D * B1 + D' * B2 \\ C &= D * C1 + D' * C2 \quad E = D * E1 + D' * E2 \end{aligned} \tag{25}$$

Where D and D' are duty ratio and its complement respectively. In order to derive state space average model including the effects of inductor dc resistance and capacitor esr, following circuits are used for subinterval one and subinterval two respectively:

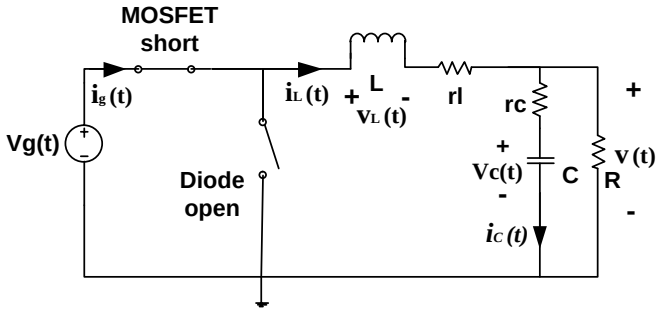

Fig. 7. *Sub Interval one*

$$0 \le t \le d(t) * Ts \tag{26}$$

$$V_L(t) = L\frac{di_L(t)}{dt} = V_g(t) - i_L(t) * rl - V(t) \tag{27}$$

$$i_C(t) = C\frac{dV_C(t)}{dt} = i_L(t) - \frac{V(t)}{R} \tag{28}$$

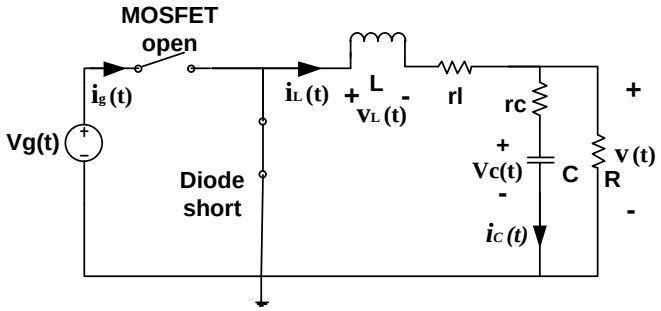

Fig. 8. *Sub Interval Two*

$$d(t) * Ts \le t \le Ts \tag{29}$$

$$V_L(t) = L\frac{di_L(t)}{dt} = -i_L(t) * rl - V(t) \tag{30}$$

$$i_C(t) = C\frac{dV_C(t)}{dt} = i_L(t) - \frac{V(t)}{R} \tag{31}$$

The output voltage V(t) is due to two state variables $i_L(t)$ and $V_C(t)$. We use superposition to obtain V(t). V(t) due to $i_L(t)$: short circuit $V_C(t)$, we use current divider rule:

$$V(t) = \frac{rc}{R + rc} * i_L(t) * R \tag{32}$$

V(t) due to $V_C(t)$: open circuit $i_L(t)$, we use voltage divider rule:

$$V(t) = \frac{R}{R + rc} * V_C(t) \tag{33}$$

$$V(t) = \frac{R}{R + rc} * V_C(t) + \frac{rc}{R + rc} * i_L(t) * R \tag{34}$$

The result coincides with the one in [8]. Replacing the value of V(t) in above equations:

$$\frac{di_L(t)}{dt} = \frac{1}{L} * V_g(t) - i_L(t) * \frac{1}{L} * (rl + \frac{R * rc}{R + rc}) - V_C(t) * \frac{1}{L} * (\frac{R}{R + rc}) \tag{35}$$

$$\frac{dV_C(t)}{dt} = i_L(t)*\frac{1}{C}*\frac{R}{R+rc} - V_C(t)*\frac{1}{C}*(\frac{1}{R+rc}) \quad (36)$$

$$A1 = \begin{bmatrix} -\frac{1}{L}*(rl+\frac{R*rc}{R+rc}) & -\frac{1}{L}*(\frac{R}{R+rc}) \\ \frac{1}{C}*(\frac{R}{R+rc}) & -\frac{1}{C}*(\frac{1}{R+rc}) \end{bmatrix}, B1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad (37)$$

For subinterval two:

$$\frac{di_L(t)}{dt} = -i_L(t)*\frac{1}{L}*(rl+\frac{R*rc}{R+rc}) - V_C(t)*\frac{1}{L}*(\frac{R}{R+rc}) \quad (38)$$

$$\frac{dV_C(t)}{dt} = i_L(t)*\frac{1}{C}*\frac{R}{R+rc} - V_C(t)*\frac{1}{C}*(\frac{1}{R+rc}) \quad (39)$$

$$A2 = \begin{bmatrix} -\frac{1}{L}*(rl+\frac{R*rc}{R+rc}) & -\frac{1}{L}*(\frac{R}{R+rc}) \\ \frac{1}{C}*(\frac{R}{R+rc}) & -\frac{1}{C}*(\frac{1}{R+rc}) \end{bmatrix}, B2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad (40)$$

$$C1 = C2 = \begin{bmatrix} \frac{R*rc}{R+rc} & \frac{R}{R+rc} \end{bmatrix}, E1 = E2 = 0 \quad (41)$$

After state matrices have been calculated, the small signal control to output transfer function can be easily calculated using the following equations [4]:

$$\frac{d\hat{x}(t)}{d(t)} = A*\hat{x}(t) + B*\hat{u}(t) + [(A1 - A2)*X + (B1 - B2)*U]*\hat{d}(t) \quad (42)$$

$$\hat{y}(t) = C*\hat{x}(t) + E*\hat{u}(t) + [(C1 - C2)*X + (E1 - E2)*U]*\hat{d}(t) \quad (43)$$

where X and U are the dc state and input matrices given as:

$X = [I_L \quad V_c]^T$ and $U = [Vg]$ (44)

We assume zero input supply disturbances and take Laplace transform of the remaining equations with following parameters:

$$A = A1 = A2,\ B = B1, B2 = 0,\ C = C1 = C2,\ E = E1 = E2 = 0 \quad (45)$$

$$s*x(s) = A*x(s) + B*U*d(s) \quad (46)$$

$$x(s)*(s*I - A) = B*U*d(s) \quad (47)$$

$$x(s) = (s*I - A)^{-1}*B*U*d(s) \quad (48)$$

Also:

$$y(s) = C*x(s) \quad (49)$$

$$\frac{y(s)}{d(s)} = C*(s*I - A)^{-1}*B*U \quad (50)$$

The above equation can be easily solved using MATLAB to obtain desired control to output transfer function.

4. Digital Control Loop

The general digital control loop implemented around a microcontroller is shown below:

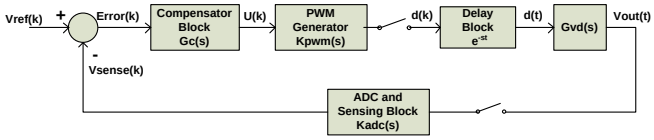

Fig. 9. *Digital Control Loop*

The output voltage is sampled by ADC at sampling frequency equal to switching frequency. The discreet error is processed by compensator and built in PWM module generates pulses with duty cycle as provided by compensator block. The modulation and processing delays are lumped in a single delay block as shown. There are various blocks in the system which are described as under:

4.1 Power Stage

The power stage of a switching regulator is modeled using either average circuit modeling approach or state space averaging approach as described in section 2 and 3 respectively. The modeling of the power stage is necessary to completely understand the dynamics of power stage and to explicitly model the effects of parasitic elements such as inductor and capacitor dc resistances. The converter transfer function Gvd(s) is usually control to output voltage transfer function, however other parameters such as inductor current can also be used as controlled variable.

4.2 ADC and Sensing Block

The output of power converter is sensed and converted using sensing and ADC block. The output voltage is generally well out of range of ADCs available in microcontrollers and DSPs and hence a voltage scaling operation is required. Although a simple voltage divider can severely affect the resolution and hence regulation accuracy [6], the need to more precisely measure the output voltage is incumbent upon two major issues. First, the requirements of the application in which the converter is operating. For example, a low output voltage converter of say 1.8 V can have strict restrictions on output voltage sensing resolution but a converter employed for lead acid battery charging or maximum power point tracking of a solar panel may not have the same stringent requirements. Second, any block after ADC needs to have effective higher resolution than the ADC itself in order to avoid limit cycle oscillations [5]. For example if ADC has resolution of 10 bits, then the PWM generator must have an effective resolution of at least 11 bits. By effective resolution one means the minimum voltage change per bit change in ADC or PWM generator. This puts restriction on the resolution of output voltage that can be achieved in practical microcontroller based systems, particularly 8 bit systems. Apart from voltage divider, the sensing part also includes a low pass filter to attenuate high frequency content in the output voltage. The low pass filter should be placed at least one half below the switching frequency. The transfer function of ADC and sensing block can be shown as:

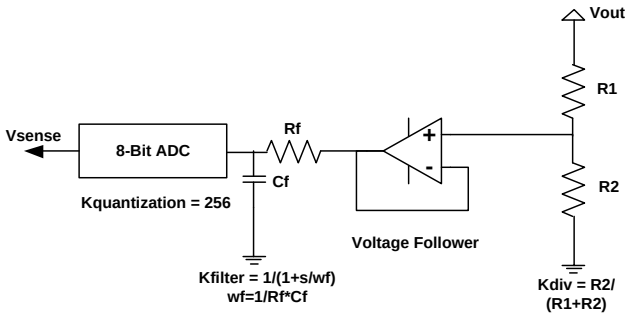

Fig. 10. *ADC and Sensing Block*

The complete gain of the sensing stage is:

$$Kadc(s) = Kdiv * Kfilter(s) * Kquantization \quad (51)$$

4.3 PID Compensator

The design of compensators for switching regulators is a well established discipline in analog domain. The transfer function of power stage is used to determine the type of compensation required, namely type 2 or type 3. PID compensators (two zeros and one integrator) have also been used to control switching regulators [5]. The advantage of PID controller, apart from its easy implementation, is the high phase boost provided by the pair of zeros as well as steady state regulation provided by single pole at origin. For these reasons, a PID regulator is a suitable choice for implementation on 8 bit microcontrollers [6]. The general transfer function of PID regulator in continuous domain is given as:

$$Gpid(s) = Kp + \frac{Ki}{s} + Kd * s \quad (52)$$

Using Euler's method, the transfer function is converted to a discreet difference equation for implementation in controller as follows:

$$d(k) = Kp * e(k) + Ki * Ts * \sum e(k) + \frac{Kd}{Ts} * [e(k) - e(k-1)] \quad (53)$$

Where e(k) is the discreet error and d(k) is the discreet duty cycle output from the PID controller. The gains of the PID compensator are selected as powers of two. This makes the implementation of PID compensator with the limited resources of an 8 bit microcontroller possible. The time taken to determine the duty cycle from equation above is critical as it directly affects the loop delay. To minimize duty cycle calculation time, shift operations are used instead of multiplication operation.

4.4 PWM Modulator

The output of the compensator block is passed to PWM generator. In microcontroller systems, the PWM generator is counter based PWM block. This puts limits on the maximum frequency and output voltage sensing resolutions. For example, if 16 MHZ clock is used to generate 100 KHZ PWM, then timer period value is 16M/100K = 160. Now, with input voltage of 20V, one bit change in duty cycle value will correspond to 20 V/160 = 125mV change in output voltage. Therefore the minimum value of output voltage change that can induce one bit change in ADC value must be greater than 125mV in order to avoid limit cycle oscillations. The value of the compensator output is so limited that the minimum and maximum values correspond to the minimum and maximum duty cycles respectively.

$$Kpwm(s) = \frac{1}{Timer\ Period\ Value} \quad (54)$$

The timer period value is dependent upon the microcontroller clock frequency for a given system.

4.5 Delay Block

In digital control loops, two types of delays are present [10]. First delay is due to ADC conversion and compensator block calculations. This delay is called computational delay. Second delay is due to the fact that any change in the value of duty cycle becomes visible only after the falling edge has occurred. This is called modulation delay. This is illustrated in following figure.

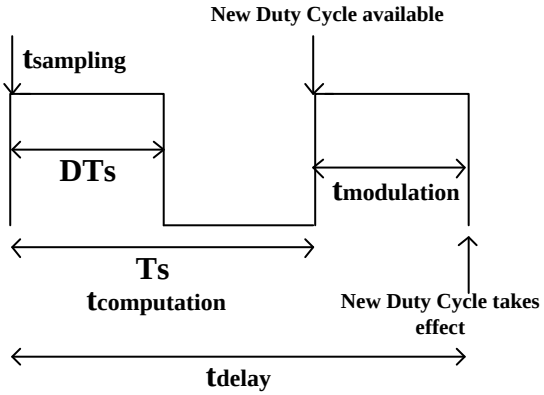

Fig. 11. *Control Loop Delays*

The above figure shows the case when entire switching cycle is required for duty cycle calculation as is the case of 8 bit systems. As can be seen, duty cycle change takes effect only after falling edge of PWM train and hence the resulting modulation delay. In 8 bit systems, the system computational power limits the time available for control law calculation as well as ADC conversion. Therefore, a complete switching cycle is dedicated to ADC conversion and duty cycle calculation. For a steady state duty cycle of 0.5, the total delay is 1.5 Ts, where Ts is the switching period. Duty cycle calculated in current switching interval is used in the next switching interval and so on.

$$Gdelay(s) = e^{-td} \quad (55)$$

4.5 Loop Gain

The complete loop gain of the system is the product of the individual gains of all the blocks that comprise the system and is given as:

$$T(s) = Gvd(s) * Kadc(s) * Gpid(s) * Kpwm(s) * Gdelay(s) \quad (56)$$

5. Buck Converter Example

In order to illustrate the steps involved in the process, a buck converter is built and controlled using STM8S microcontroller. STM8S series microcontrollers are 8 bit microcontrollers from ST Microelectronics which incorporate many useful peripherals among which one is of principle importance to the implementation of a digital control loop. The STM8S controllers incorporate very fast ADC with conversion times equal to 2.5us. This is by far the fastest ADC in knowledge of

the author, available in any 8 bit microcontroller system. The ADC has a fixed 10 bit resolution. This can be a detrimental keeping in view the fact that PWM resolution at 100 KHz switching frequency is lower than 10 bits. However, using external voltage divider and by compromising on output voltage resolution (contingent upon application), one can avoid limit cycle oscillations. The following table shows the buck converter parameters used to demonstrate the example:

Table 1 *Buck Converter Parameters*

Vin	20V
Vout	10V
Iout	1A
L	470uH
RL	15e-3Ω
C	220µF
Rc	10e-3Ω
Ts	10µs
R1/R2	20
Rf	1e3 Ω
Cf	10e-9F

The schematic diagram of the system is shown next:

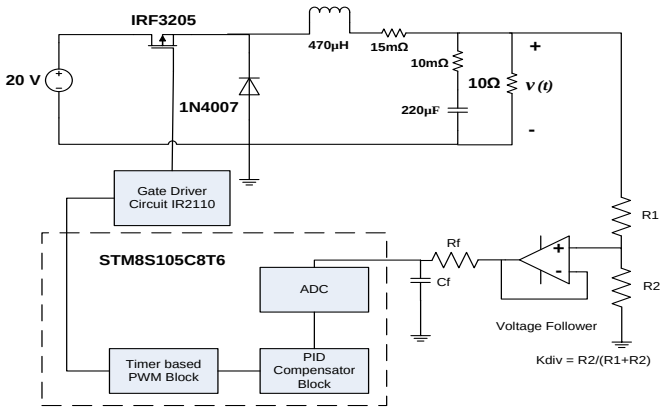

Fig. 12. *Schematic of Buck Converter Controlled by STM8S*

5.1 MATLAB Simulation

The transfer functions of the various blocks are provided next:

$$Gvd(s) = \frac{0.0004 * s + 200}{9.409e^{-7} * s^2 + 0.00052 * s + 10.02} \quad (57)$$

$$Kadc(s) = \frac{5.1e^6}{s + 1e^5} \quad (58)$$

$$Kpwm(s) = 0.00063 \quad (59)$$

$$Gdelay(s) = e^{-1.5*Ts} \quad (60)$$

The uncompensated Loop gain is obtained by setting compensator transfer function to unity:

$$Tu(s) = Gvd(s) * Kadc(s) * Kpwm(s) * e^{-1.5*Ts} \quad (61)$$

$$Tu(s) = e^{-1.5e-5*s} \frac{12.75 * s + 6.375e^6}{9.409e^{-7} * s^3 + 0.0946 * s^2 + 62.02 * s + 1e^6} \quad (62)$$

The bode plot of the uncompensated loop gain is obtained in MATLAB.

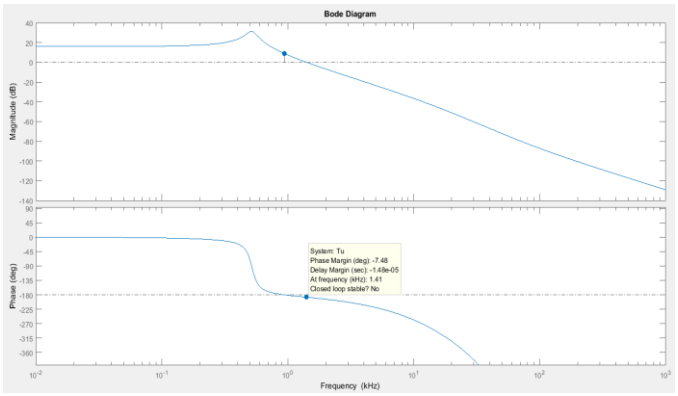

Fig. 13. *Bode Plot - Uncompensated System*

The phase margin comes out to be -7.48°. It should be emphasized here that by using an 8 bit microcontroller, the main parameter of interest is the phase margin of the system. The bandwidth of the system is of secondary importance as the proposed applications of this particular converter do not require very fast speed of the control loop. We select the zeros of PID controller as shown below:

$$Gpid(s) = \frac{0.125 * s^2 + 64 * s + 16}{512 * s} \quad (63)$$

The resulting bode plot of the compensated system is shown below:

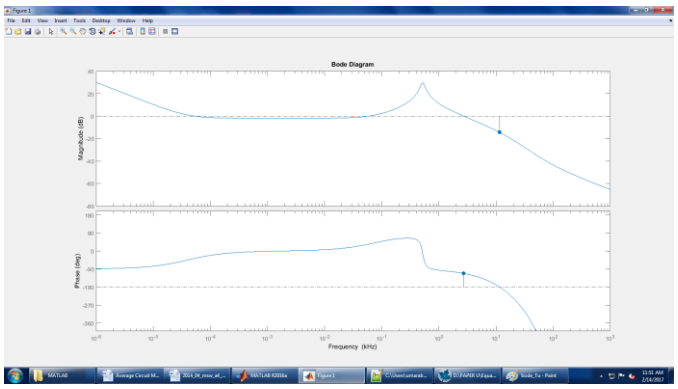

Fig. 14. *Bode Plot - Compensated System*

The gain margin comes out to be 68° with a cutoff frequency of 2.7 KHz. It should be noted that the zeros of PID controller are selected such that after simplification, the individual gains Kp,Ki and Kd come out to be powers of 2 which helps in implementation.

5.2 Practical Implementation

The proposed controller is implemented on an STM8S microcontroller. The software for the controller is developed in Code Block IDE and SDCC compiler which are both freely

available. Although assembly language implementation provides much faster code, implementation in C language is far easy and practical and is used for this application. A timer available in the STM8S controller is used to generate duty cycle controlled PWM waveform as well as implement compensation algorithm. The timer is configured for PWM of 100 KHz with interrupt on the timer overflow event, which is the event at which the timer starts recounting. In interrupt service routine, ADC conversion of output voltage and compensation algorithm are implemented sequentially. The duty cycle can only be updated at the beginning of the timer cycle. Therefore, a complete switching cycle is dedicated for ADC conversion and control law implementation. This is the worst case scenario and is inevitable in an 8 bit controller with very limited computational power. However with proper implementation, it can still provide acceptable performance.

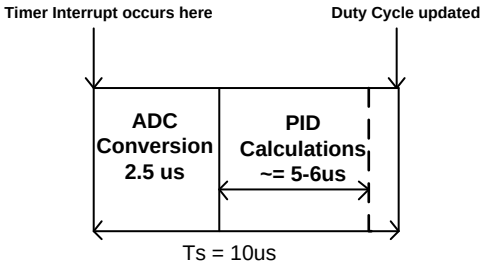

Fig. 15. *Timer ISR Operations*

The flowchart of the main ISR used to implement the controller is shown below:

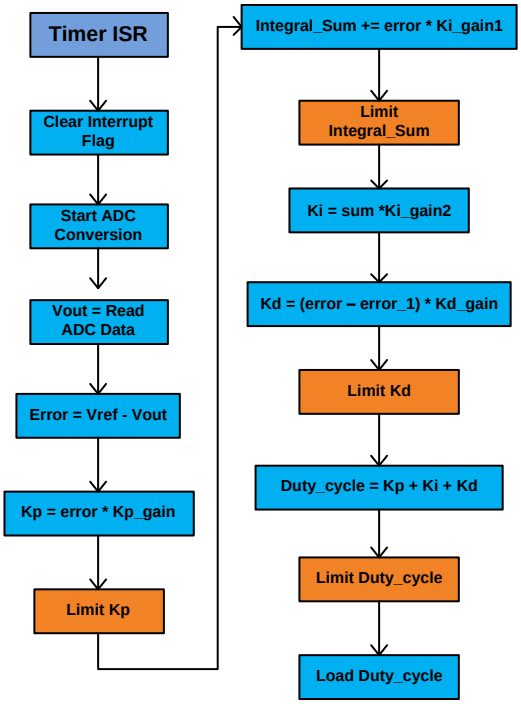

Fig. 16. *Timer ISR*

All the variables used in the software are signed or unsigned integers. The programmer should take care of implicit conversion between signed and unsigned conversions as this can lead to hard to track errors. In 8 bit systems, the computational power as well as time available for control loop is limited, therefore simple integers are used instead of number representations which are more suitable for high speed DSPs. Also it should be noted that the controller outputs Kp, Ki and Kd are limited in addition to duty cycle limits. Such limits do effect the controller behavior but are necessary for practical reasons such as noise and register over runs. Such limits should be decided dynamically after practical measurements and observations. Apart from this, it should be noted that gain such as Ki is implemented in stages. This is done because it results in more stable operation as observed practically. The practical setup on bread board along with STM8S discovery kit is shown next:

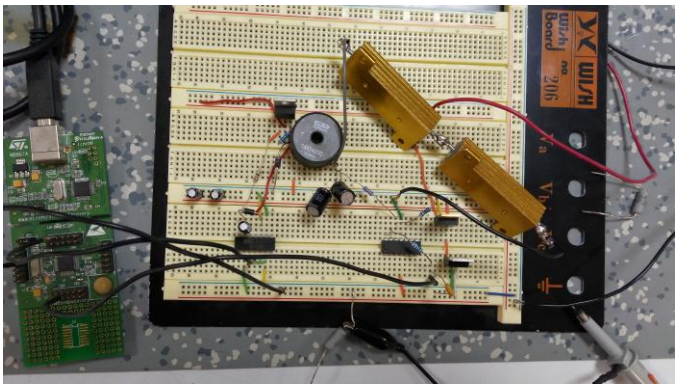

Fig. 17. *Practical Setup*

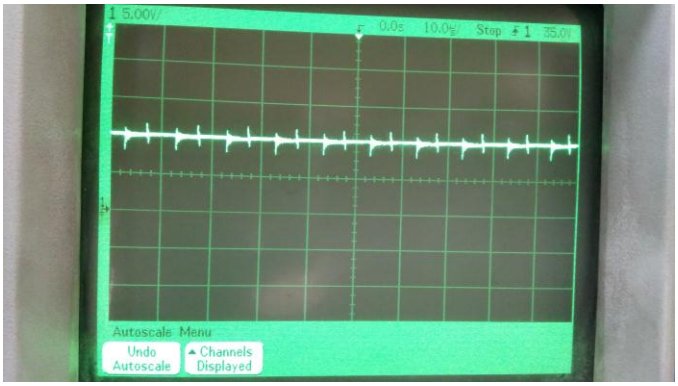

Fig. 18. *Steady State Output Voltage*

As can be observed, the output voltage is steady at a constant level without limit cycle oscillations.

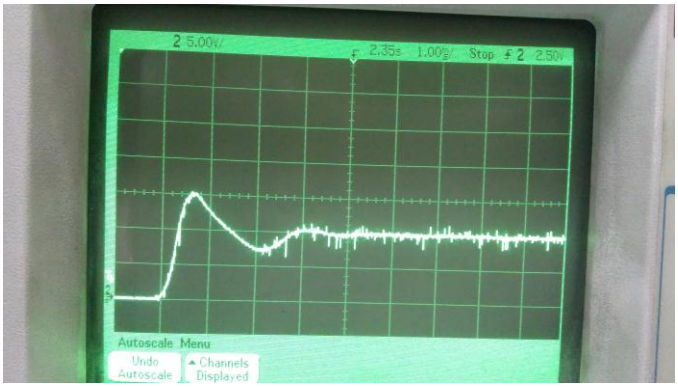

Fig. 19. *Startup Response*

It can be seen that the output voltage settles at desired level with approximately 50% overshoot and in almost 3ms. This may be less than the predicted bandwidth of the controller, however, is still sufficient for the target application areas as discussed next. The decrease can be attributed to the limited

on the actual gains in controller implementation which are necessary due to practical reasons.

6. POTENTIAL APPLICATIONS

This paper presented a digitally controlled buck converter using an 8 bit microcontroller. One might wonder the scope of applications where this controller might be used. Although analog and DSP based digital controllers provide far better dynamic and steady state performances and have been well established, yet not every application warrants use of such costly (DSP based) or inflexible (analog) solutions. Ease of implementation, flexibility and low cost are the key merits of this 8 bit microcontroller based converter. Potential applications can be battery charging, maximum power point tracking, dc-dc converters in ups applications (12V to 400 V converters). Although an 8 bit controller with 16 MHZ clock was used for this application, the system clock in 8 bit systems can be increased upto 48 MHZ which can provide further performance boost and flexibility in human machine interface implementation. Moreover, in this application, 100KHZ was the switching frequency selected for buck converter which is a reasonable frequency for most dc-dc converter applications.

7. CONCLUSION

This paper presented mathematical modeling of a buck converter including the effects of parasitic such as inductor dc resistance and capacitor esr. A sampled data model of digitally controlled buck converter system was derived next. A suitable PID controller was selected to obtain the satisfactory control loop performance. MATLAB simulation and practical implementation results were presented to validate the theoretical work. It is believed that such low cost controller can be successfully employed in battery charging and similar applications.

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