9-Level Cascaded Switched-Diode Multilevel Inverter For Renewable Energy Integration

R Jenin Prabhu, V. Surya, Balaji L. Hegde, D. Balaji

Abstract: In this paper, a new topology of two-stage cascaded switched-diode (CSD) multilevel inverter is proposed for medium voltage renewable strength integration. Firstly, aims to limit the number of switches along with its gate drivers. Thus, the installation space and fee of a multilevel inverter are reduced. The spike removal switch added in the first stage of the inverter gives a flowing direction for the reverse load current, and as a result, excessive voltage spikes going on at the base of the stepped output voltage based upon conventional cascaded switched-diode multilevel inverter topologies are removed. Moreover, to resolve the problems related to DC source fluctuations of multilevel inverter used for renewable power integration, the clock section shifting (CPS) one-cycle control (OCC) is developed to control the two-stage CSD multilevel inverter. By shifting the clock pulse section of every cascaded unit, the staircase-like output voltage waveforms are obtained and a strong suppression capacity against fluctuations in DC sources is achieved.

Index Terms: Energy storage, DC micro grids, Novel Cascaded multilevel inverter, renewable energy, one-cycle control, single inductor, Three-port converter, two-stage.

1. INTRODUCTION

Various multilevel inverter topologies have been proposed in the previous decade, which have been significantly studied for renewable electricity integration structures [1-3]. Fig. 1 indicates the block graph of a renewable power generation machine using a multilevel inverter. It integrates a variety of renewable sources, such as photo voltaic energy, wind energy, tide energy and so on and they are connected to a converter to generate DC power, which is saved in a capacitor or battery. After related to a multilevel inverter, DC power is converted into AC power. It is evident that the multilevel inverter capable of converting a single DC voltage source from a capacitor or battery into an AC voltage source is a key thing of most stand-alone renewable energy technology systems. The multilevel inverter topologies, in general, can generate high satisfactory voltage waveforms, where energy switches are operated at a very low frequency [4] [5]. The basic topologies of the present multilevel converters are divided into three types: the cascaded multilevel inverter topology [6], [7], the diode clamped multilevel inverter topology and the flying capacitor multilevel inverter topology. Among these L. Wang, Q. H. Wu and W. H. Tang are with School of Electric Power Engineering, South China University of Technology, Guangzhou 510641, China. Corresponding creator is Professor W. H. Tang, E-mail: wenhutang@scut.edu.cn, Tel: 0086 020 87112999. The work is supported by means of Guangdong Innovative Research Team Program (NO. 201001N0104744201) and the Fundamental Research Funds for the Central Universities (NO.2017BQ045).

• Mr. R Jenin Prabhu, Asst prof, EEE department, Vel Tech, Avadi, Chennai, Email: jeninprabhu@veltechengg.com
• V. Surya, EEE department, Vel Tech, Avadi, Chennai, India, Email: Suryakarthi97@gmail.com
• Balaji L. Hegde, EEE department, Vel Tech, Avadi, Chennai, India, Email: balajihedge10630@gmail.com
• D. Balaji, EEE department, Vel Tech, Avadi, Chennai, India, Email: devabala40@gmail.com

Fig.1. Renewable energy Generation System With Multilevel Inverter.

Topologies, the cascaded multilevel converter has attracted extra attention due to its simple structure and character DC electricity sources for every cascaded unit. It has first-rate plausible to be employed in renewable strength generation systems, such as solar energy, wind energy, gas cells. The traditional cascaded multilevel inverter topology is the cascaded H-bridge (CHB) multilevel inverter, and the foremost disadvantage of the CHB topology is the requirement of a excessive variety of switches and its associated gate drivers, which can also lead to an luxurious and complicated average system. Therefore, several new multilevel inverter topologies using a decreased wide variety of switches and associated gate drivers were developed in recent years. Among them, a cascaded half-bridge topology proposed via efficaciously reduced nearly half the wide variety of required switches in contrast with the CHB topology. Then, Rasoul Shalchi Alishead proposed a cascaded switched-diode topology. Compared with the cascaded half-bridge topology, it can produce greater voltage degrees with a much less range of switches. However, due to the lack of a course for reverse load currents, under a R-L load, excessive voltage spikes happen at the base of the
stepped output voltage, which tend to deteriorate power quality. This paper affords a novel two-stage CSD multilevel topology, accomplishing a greater wide variety of voltage degrees with a lower wide variety of switches, which additionally eliminates excessive voltage spikes below R-L masses by using a course for reverse load currents.

Meanwhile, the generally used modulation techniques for cascaded multilevel inverters are quintessential frequency manipulate method, The service based sinusoidal PWM (SPWM), the area vector modulation (SVM) and some nonlinear modulation methods, such as hysteresis control sliding mode control and so on. However, in a renewable strength integration system, DC electricity sources of a multilevel inverter are supplied via the renewable energy generation, as shown in Fig. 1. In practice, the DC grant is always with fluctuation because of all kinds of complex factors. For instance, outputs of photo voltaic cells exchange in positive vary following editions of light intensity, temperatures, and so on, which show up as an output mixed with low frequency ripples. When using such a DC furnace as the enter of multilevel converters, conventional modulation strategies are unable to meet the want of industrial applications. Hence, there is a necessity to strengthen a widespread manage method with an accurate static overall performance and a sturdy suppression capability towards the interference in DC sources. In this paper, a CPS OCC method is developed for controlling the proposed CSD multilevel topology. By transferring the section of the triggering clock pulses of each cascaded unit, the staircase-like output voltage waveforms are acquired and a strong inhibition potential against the interference in DC sources is achieved. The paper is organized as follows: The proposed two-stage CSD multilevel topology is added in Section 2, and the benefits of the two-stage CSD topology are validated compared with the CHB and cascaded half-bridge topologies in Section 3 illustrates the layout and implementation strategies of the CPS OCC method. In Section 4 and 5, simulation and experimental effects are presented. The conclusions are drawn in Section 6.

2 TOPOLOGY OF THE PROPOSED TEO-STAGE CSD MULTILEVEL INVERTER

The above discern which consists of a n cascaded switched-diode converter with one spike elimination change Sg and a full-bridge inverter, the place n is the wide variety of the cascaded fundamental units. The primary unit 1 as shown in Fig. 2 consists of a DC voltage source (or a capacitor with a DC voltage equal to u1), a switch S1 with its inside reverse diode and a diode D1. It is clear that the parallel connection of the diode D1 avoids the shoot-through phenomenon of a bridge arm. Two values can be obtained for u1 of the basic unit 1, which are u1 when switch S1 conducts and 0 when switch S1 is grew to become off. The spike elimination change Sg, related between unit 2 and unit n, provides a flowing direction for the reverse load current. When S1 is on, S21 • • • Sn1 off, Sg is grew to become off.

\[ N_{\text{level}} = 2n + 1 \]  
\[ N_{\text{IGBT}} = n + 5 \]

(1) and (2)

The cascading sketch of n simple devices and Sg structure the first stage, as shown in Fig. 2. The maximum output voltage of the first stage is given as follows: \( u_g = u_{o1} + u_{o2} + \cdots + u_{on} \). (1) and for states of switches S11, S21, • • • , S(n−1)1, Sn1, 2 n one-of-a-kind values of \( u_g \) are obtained, as listed in TABLE I.

<table>
<thead>
<tr>
<th>State</th>
<th>Switches states</th>
<th>( u_{o1} )</th>
<th>condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>on off off off on</td>
<td>( u_k )</td>
<td>( u_{ref} &gt; 0 )</td>
</tr>
<tr>
<td>2</td>
<td>off on on off on</td>
<td>( -u_k )</td>
<td>( u_{ref} &lt; 0 )</td>
</tr>
</tbody>
</table>

(3)

As proven in TABLE I, the first-stage converter can generate positive staircase-like output voltage waveforms. For producing both positive and terrible output voltages, the 2d stage converter is needed.

3 COMPARISON WITH TOPOLGIES OF CHB AND CASCADED HALF-BRIDGE

The CHB topology consists of n DC sources or cells every related to a H-bridge inverter, as shown in Fig. 3. Each H-bridge can generate three ranges of voltage output, i.e, udc, 0 and −udc, respectively. Under the symmetric case, the wide variety of the required switches for a Nlevel output voltage is derived as follows: NIGBT.

\[ N_{\text{IGBT}} = \frac{N_{\text{level}} + 9}{2} \]

(3)

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\[ u_{\text{device}} = \sum_{i=1}^{n} u_{\text{switch} \cdot i} + \sum_{j=1}^{n} u_{\text{diode} \cdot j} \]

(4)
4 THE PROPOSED CPS OCC METHOD FOR THE TEO-STAGE CSD MULTILEVEL INCERTER

4.1 The design of CPS OCC

Compared with the CHB topology, a cascaded half-bridge topology proposed correctly reduces almost half the range of switches, as proven in Fig. 4. It is composed of a \( n \) cascaded half-bridge converter and a full-bridge inverter. Under the symmetric case, the wide variety of the required switches for a \( N \) level output voltage is derived as follows:

\[
\text{NIGBT} = N_{\text{level}} + 3
\]

Another necessary issue in designing a multilevel converter is the rating of switches. Therefore, the contrast of the energy factor requirements among the CHB, the cascaded half-bridge and the proposed CSD topologies is listed. Concerning the variety of required switches and voltage rating of all the gadgets (switches and diodes). Based on (4), (5) and (6), the variety of required switches and drivers for realizing \( N_{\text{level}} \) voltages for output are in contrast. Fig. 5 illustrates the results of the assessment NIGBT towards \( N_{\text{level}} \) from specific points. As the discern shows, underneath the symmetric case, the CSD topology requires a much less range of IGBTs and its related gate drivers for realizing \( N_{\text{level}} \) output voltage. For instance, to generate a 21-level output voltage, the CSD topology (Point 3) wants 15 IGBTs/drivers. However, the CHB topology (Point 1) and cascaded half-bridge topology (Point 2) require forty IGBTs/drivers and 24 IGBTs/drivers, respectively. Although there are 10 diodes added in the proposed topology, the required range of the IGBTs and its related gate drivers.

4.2 The implementation of CPS OCC

CPS OCC is implemented with simple logic functions (comparison and integration) as shown in Fig. 6. Here, the implementation for control of primary unit 1 is described as follows: the integration technique starts at the moment when \( S_{11} \) is became on with the aid of a fixed frequency clock pulse. At this moment, \( u_{o1}(t) = u_1(t) \). As time goes on, the integration price \( u_{\text{int}1}(n) \) will increase from its preliminary value, and \( u_{\text{int}1}(t) \) is in contrast with the control reference \( u_{\text{ref}1} \) instantaneously. At the instantaneous when \( u_{\text{int}1}(t) \) reaches \( u_{\text{ref}} \) the comparator generates a reset pulse to reset the RS flip-flop (\( Q = 0 \)). Then \( S_{11} \) is modified from the on-state to off-state. At the identical time, the integrator is reset to zero. At this second \( u_{o1}(t) = 0 \) Switch \( S_{11} \) is off until the arrival of the next clock pulse, which begins the \((n + 1)\)th switching cycle. As the diagram and implementation for other cascaded fundamental gadgets are similar to that of unit 1, the small print of other gadgets are no.
5 CIRCUIT OPERATION PRINCIPLE

As the proposed NITPC has two bi-directional ports, namely, the battery port and the DC bus port, it increases the mixtures of different electricity flow patterns among the three ports. Overall, the proposed converter is capable of running in seven distinct modes based on the electricity stipulations of every port coupled with the battery voltage stage which is used to consider its country of charge. In DC micro grid application, the aforementioned seven operation modes can be split into grid-connected mode and islanded mode. In grid-connected mode, the DC bus is treated as a modern-day reversible load, which can both take in or provide power. Modes 1 to 5 belong to this group.

6 EXPERIMENTAL VERIFICATIONS

6.1 Block diagram

Verification of the Operation Modes Switching
1) Load switching for PV (Mode 2 to Mode 1): Fig. 9(a) indicates the alternate in ingesting masses and the enter PV electricity stays unchanged. This state of affairs takes place when the PV power is limited (e.g. at dusk) to grant the DC bus whilst the battery is not in full SOC (e.g. battery self-discharge). It will therefore dispatch electricity to the battery. As can be seen, Vpv and ipv are preserved whilst idc and ib indicate the modern-day float switches from DC bus to battery. Moreover, the alternate between these two modes can be easily carried out by means of switching S2. 2) DC bus charges Battery with the bus unexpected starts offevolved to require strength (Mode 4 to Mode 7): This scenario takes place when the DC microgrid adjustments from grid-connected mode to islanded mode, for instance power reduce at night time. In order to affirm the practicability of the bi-directional operations between the two ports, the transient response is shown in Fig. 9(b). Duty cycles d1 and d3 set the on-time for switches S1 and S3 respectively. This indicates a alternate of operation from

7 CONCLUSION

A novel single-inductor NITPC is proposed for a PV battery-DC microgrid. A more flexible power glide can be executed as two of the three ports are capable of managing reversible
currents as compared to one bi-directional port in present NITPCs. Moreover, an extra compact layout is realized barring the usage of the transformers and full-bridge converters in isolated TPCs which are the common options to combine a bi-directional load. The proposed NITPC can work and transit easily between DC grid-connected mode and islanded mode. Detailed operation principles, modes choice necessities and manage techniques are explained. The converter can be reconfigured as SISO, SIDO or DISO converter in accordance to the selected mode. A assessment of the proposed NITPC with two separate converters is given. Experimental outcomes are given and demonstrated the flexible operation of the converter.

REFERENCES
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