Soft Switched Stepped Dc-Dc-Ac Hybrid Converter

R. Uthisamay, J. Karpagam, V. J.Vijayalakshmi, P. Ravikumar

Abstract: In this paper topologies of Soft Switched Hybrid Multilevel Converter (SSHMLC) and Soft Switched Hybrid Multilevel Boost Converter (SSHMLBC) are designed and developed for mitigating power quality issues such as harmonics, voltage stress and power spectral density at the multiples of switching frequency. The proposed systems consist of the boost power converter module, snubber/soft switching module and H-bridge inverter configuration. To highlight the importance of the proposed converter, a comparative analysis is made with existing Two-Level Voltage Source Inverter (TLVSI), Boost Two-Level Voltage Source Inverter (BTLVSI) and the significant features are investigated for solar PV applications. Multi Carrier Sinusoidal Pulse Width Modulation (MCSPWM) technique is developed and implemented for the switching of SSHMLC and SSHMLBC. To mitigate power quality issues, optimized firing pulses are generated using MCSPWM algorithm and the equivalent embedded C coding is fetched into micro controller. Individual voltage and current harmonics have been analyzed for various load conditions. The proposed inverter model is simulated using MATLAB/SIMULINK software and the results are validated through experimentation.

Index Terms: DC to DC converter, multicarrier sinusoidal pulse width modulation, power converters, power quality issues, stepped DC Link converter, total harmonic distortion, zero voltage switching module.

1 INTRODUCTION

In recent years, power electronics have been one of the most focused areas in research and development sectors. Different configurations of power converters and optimizing techniques are developed to interface the renewable resources with stand alone and grid connected electrical load systems. One of the limitations of the traditional two level inverter switches are forced commutated due to voltage stress. To reduce voltage stress across the inverter switches, additional resonant soft switching circuits are required [1]. In addition to this, to reduce voltage stress Multilevel Inverter (MLI) configurations are also considered as a new breed of power converter options for high power applications [2]-[11]. To reduce power components in MLI and improve power quality profile in two-level inverter, SSHMLC topologies are developed in combination with the two-level inverter and CMLI [12]-[17]. To obtain quality of power output, power electronics engineers have paid great attention to SSHMLC and its boost circuits as a new kind of power converter. SSHMLBC is not only used for achieving higher power rating but also acts as soft switching module for high power converter. The DC input voltage is boosted to the nominal voltage level by the boost chopper network. This results in reduction of magnetic component like transformer, number of DC sources and power switches. The motivation of the proposed work is to design and analyze the performance of SSHMLC and SSHMLBC with conventional inverter systems, thereby reducing the voltage stress, harmonics, switching loss and filter components.
drastically reduced. For every increase in levels, only one switch is get added.

Fig. 1. Generalized structure of SSHMLC system

B) Modes of Operation of SSHMLC

The output voltage magnitude in mode 1 and 4 operations is expressed using equations (3) and (4)

\[ V_1 = V_{dc1} \] (For Positive Cycle) \hspace{1cm} (3)

\[ V_1 = -V_{dc1} \] (For Negative Cycle) \hspace{1cm} (4)

The output voltage magnitude in mode 2 and 5 operation is given using equations (5) and (6)

\[ V_2 = V_{dc1} + V_{dc2} \] (For Positive Cycle) \hspace{1cm} (5)

\[ V_2 = -(V_{dc1} + V_{dc2}) \] (For Negative Cycle) \hspace{1cm} (6)

The magnitude of AC output voltage in mode 3 and 6 operation is given by equations (7) and (8)

\[ V_o = V_{dc1} + V_{dc2} + V_{dc3} \] (For Positive Cycle) \hspace{1cm} (7)

\[ V_o = -(V_{dc1} + V_{dc2} + V_{dc3}) \] (For Negative Cycle) \hspace{1cm} (8)

Table 1

<table>
<thead>
<tr>
<th>Levels</th>
<th>DC Link Module</th>
<th>Inverter</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>ON, OFF</td>
<td>ON, OFF</td>
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<tr>
<td>2</td>
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<td>S1, S2, S3</td>
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<td>D1, D2, D3</td>
<td>S1, S2, S3</td>
</tr>
<tr>
<td>4</td>
<td>S1, S2, D3</td>
<td>S1, S2, S3</td>
</tr>
<tr>
<td>5</td>
<td>S1, S2, D3</td>
<td>S1, S2, S3</td>
</tr>
<tr>
<td>6</td>
<td>S1, S2, S3</td>
<td>S1, S2, S3</td>
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3 PERFORMANCE ANALYSIS OF TWO LEVEL AND SOFT SWITCHED HYBRID MULTILEVEL CONVERTER WITH AND WITHOUT BOOST SYSTEM

A) Two-Level Inverter System

The entire circuit is simulated using SIMULINK tools and its performance has been investigated. The present model of TLVSI fed AC load system is indicated in Fig. 3. Fig. 4 shows the output voltage \( (V_m=325 \text{ V}) \) of two-level inverter fed RL load system. The variations of spectral density for the output voltage of BTLVSI fed RL load system is indicated in Fig. 5. The switching frequency of two-level inverter is considered to be 2 kHz. The estimation of power spectral density for the output voltage of TLVSI in the multiples of switching frequency like 2 kHz, 4 kHz, 6 kHz and 8 kHz are 28 dB/Hz, 22 dB/Hz, 20 dB/Hz and 18 dB/Hz respectively. From the PSD analysis, it is implied that the concentration of power is maximal in the manifolds of switching frequency which causes enhanced switching losses. Also, the analysis clearly elucidate that the two-level inverter system has high switching stress.

Fig. 3. Simulation model of TLVSI fed AC Load System

Voltage harmonics in the multiples of switching frequency is scrutinized using FFT algorithm as indicated in Fig. 6. The voltage harmonics magnitude in the switching frequency like 2 kHz, 4 kHz, 6 kHz and 8 kHz of TLVSI are 76 V, 44 V, 28 V and 24 V respectively. From the harmonic review, it is implied that the TLVSI has elevated power loss in various switching frequency.
B) Boost Two-Level Voltage Source Inverter System

The pretense replica of BTLVSI system is indicated in Fig. 7. The entire circuit is simulated using SIMULINK tools and its concert has been investigated. The power spectral thickness for the output voltage of BTLVSI fed drive load system is exposed in Fig. 8. The switching frequency of two-level inverter is 2 kHz. At 2 kHz, the power spectral density for the output voltage of BTLVSI fed drive load is 28 dB/Hz. Similarly, at 4 kHz, the power spectral density for the output voltage of BTLVSI fed drive load is 24 dB/Hz. From the PSD analysis, it is understood that the density of power is maximum at the multiples of switching frequency which leads to more switching loss. Also, the analysis clearly elucidate that the two-level inverter system has high switching stress. Voltage harmonics at the manifolds of switching frequency has been inspected using FFT algorithm. The voltage harmonics at the switching frequency of BTLVSI fed drive load arrangements are indicated in Fig. 9. At 2 kHz, the enormity of voltage harmonics of BTLVSI fed drive load is 72 V. correspondingly, at 4 kHz, the enormity of voltage harmonics of BTLVSI fed drive load is 42 V. From the harmonic investigation, it is implicated that the BTLVSI has elevated power loss at the manifolds of switching frequency.

Fig. 5. Output Voltage Power Spectral Density of TLVSI

Fig. 6. Voltage Harmonics at the Switching Frequency of TLVSI

Fig. 7. Simulation model of BTLVSI System

Fig. 8. Output Voltage Power Spectral Density of BTLVSI fed Drive Load

Fig. 9. Voltage Harmonics at the Switching Frequency of BTLVSI fed Drive Load

Fig. 10 shows the experimented output voltage of BTLVSI fed drive system. The obtained result has the voltage magnitude and frequency of 240 V, 50 Hz respectively. The power spectral density for the experimented output voltage of BTLVSI fed drive load system is indicated in Fig. 11. At 2 kHz, the power spectral density for the output voltage of BTLVSI fed drive load is 36 dB/Hz. Similarly, at 4 kHz, the power spectral density for the output voltage of BTLVSI fed drive load is 28 dB/Hz.

Fig. 10. Experimented Inverter Output Voltage of BTLVSI fed Drive Load
The proposed model of seven-level SSHMLC fed RL load system is indicated in Fig. 12. Three symmetrical DC sources (108.5 V each) are connected with respective DC link circuits. The outputs of DC link modules are contemporized with inverter system. The output voltage of DC link circuit is revealed in Fig. 13. From the waveform, it is presumed that the DC link voltage is synthesized with stepped DC voltages. Output voltage (V_m=325 V) and load current of SSHMLC is implicated in Fig. 14 and Fig. 15 correspondingly. The power spectral density for the output voltage of SSHMLC fed RL load system is indicated in Fig. 16. The power spectral density for the output voltage of SDCL in the manifolds of switching frequency like 2 kHz, 4 kHz, 6 kHz and 8 kHz are 18 dB/Hz, 10 dB/Hz, 4 dB/Hz and 2 dB/Hz respectively. From the PSD investigation, it is related with TLVSI configurations, the intended SSHMLC system has mitigated power density in the manifolds of switching frequency. Also, the review clearly elucidate that the two-level inverter system has elevated switching stress. Voltage harmonics in the manifolds of switching frequency is scrutinized using FFT algorithm as shown in Fig. 17.
The pretense model of seven-level solar PV fed SSHMBC fed R load system is specified in Fig. 18. Solar PV panels are modeled for 48 V and its output voltage is boosted to 108.5 V by employing boost chopper. Output of boost chopper units I, II and III are related with relevant DC link circuits. The outputs of DC link section are synced with inverter system. The power spectral density for the output voltage of BTLVSI fed drive load system is indicated in Fig. 19. The switching frequency of SSHMBC is 2 kHz. At 100 kHz, the power spectral density for the output voltage of BTLVSI fed drive load is 20 dB/Hz.

Output voltage of the seven-level SSHMHL system is indicated in the Fig. 22. From the obtained result, it is inferred that the output voltage and the frequency of the SSHMHL is 33.08 V and 49.33 Hz. The experimental voltage FFT spectrum of seven-level SSHMHL is indicated in Fig. 23. From the spectrum it is inferred that the seven-level SSHMHL system has reduced voltage stress in the multiples of switching frequency.
SSHMLC and SSHMLBC are well suited for solar PV integrated high power stand alone and grid connected systems.

REFERENCES


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Fig. 23. Experimental Output Voltage FFT Spectrum of SSHMLC

Fig. 24. Comparative analysis- power spectral density

4 COMPARATIVE ANALYSIS

To emphasize the merits of the proposed system, comparative analysis are carried out with respect to power distribution over a wide range of frequency. PSD analysis is made at the multiples of switching frequency such as 2 kHz, 4 kHz, 6 kHz and 8 kHz. From the analysis, it is inferred that, compared to TLVSI and BTLVSI, the proposed SSHMLC and SSHMLBC topologies and have the reduced power density of 9 dB/Hz, 10 dB/Hz, 10 dB/Hz and 11 dB/Hz respectively in the multiples of switching frequency. Thus the reduced switching losses and switching stress in the proposed system are validated. Similarly, the average harmonic content of the output voltage of TLVSI and proposed SSHMLC in the multiples of switching frequency are 43 V and 14.75 V respectively. From the analysis, it is understood that the proposed system has 65.7 % reduced average harmonic content in the output voltage.

5 CONCLUSION

The proposed topology intensively focussed the power the power quality issues and voltage stress across the inverter switches. In this paper, four inverter configurations (TLVSI, BTLVSI, SSHMLC and SSHMLBC) are investigated through pretense models and hardware experimentation. Output voltage of SSHMLC has reduced harmonic content over TLVSI. Proposed seven-level converter has 33.33 % reduced switch count over conventional CMLI seven-level configurations. The proposed topologies of SSHMLC and SSHMLBC are well suited for solar PV integrated high power stand alone and grid connected systems.


