Low Voltage Low Power Current Comparator Using Dtmos

Narendra Pratap Sharma, Maneesha Gupta

Abstract: In this paper we have proposed a novel ultra-low power current comparator which is based on Dynamic Threshold Metal Oxide Semi-conductor (DTMOS) technique to reduce the power dissipation which is achieved by reducing the supply voltage. The Circuit has been implemented at supply voltage as low as ±0.3 V and in 0.18 µm (Taiwan Semiconductor Manufacturing Company) TSMC technology parameters.

Keywords: current comparator,

I. Introduction

Nowadays the size of the transistor is reducing, because of this reduced size of MOS transistor, it demands the lower supply voltage [1]. In fields of biomedical devices like hearing aids requires minimum sized batteries, that is why we requires low voltage low power ckt design. This can be achieved by reducing the supply voltage, but it can affect signal quality and voltage gain. Due to reduction in supply voltage there is a reduction in dynamic range hence degradation in signal quality. Further, scaling CMOS with scaling factor $\alpha < 1$, deteriorates output resistance of MOS transistor, due to which maximum achievable gain also reduces from a MOS Amplifier.. So we need new techniques to achieve this purpose. Many LVLP (Low Voltage Low Power) techniques have been developed in CMOS technology [2-6]. One of the LVLP term is DTMOS (Dynamic Threshold MOS) transistor .DTMOS was first suggested by [7-8]. DTMOS transistor have the ability to dynamically regulate the Threshold Voltage of transistor, using body biasing technique. Various circuit hence been proposed by applying this technique [9-15].

II. Basic current comparator concept

A current comparator is used to determine if a given current signal exceeds a given threshold and produces an output voltage accordingly. It receives an input current and compares it to a pre-defined threshold current and produces output in the form of a voltage. An ideal current comparator should allow the input signal to settle quickly, or there would be no capacitance on the input side and it should be able to take an infinitely small change in current and convert it into voltage at the output of the device. Working of Current Comparator is as follows:-

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$$V_{out} = +ve\ if\ I_{in} > I_{ref}$$
$$V_{out} = -ve\ if\ I_{in} < I_{ref}$$

Transfer characteristics of an ideal current comparator are shown in the Fig 1.

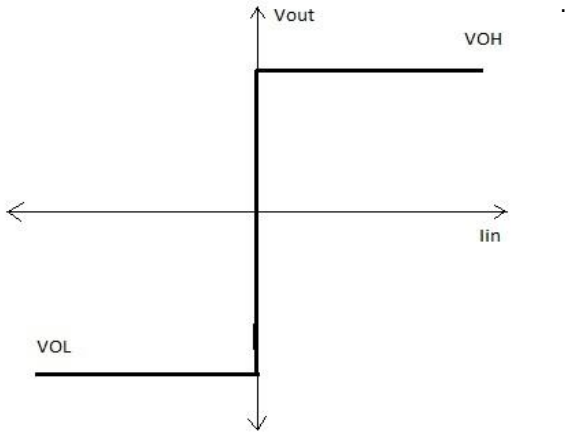

Figure 1 *Transfer Characteristics of an Ideal Current Comparator*

V_{OH} and V_{OL} in the figure signifies the capped values of the logical output states. There are three stages of a current comparator:

(1). Input stage (Current Differencing Stage)
(2). Mid stage (Gain Stage)
(3). Final stage (Output Stage)

We here only discuss about the Gain Stage and Output stage.

III. DTMOS

The concept of DTMOS was first introduced in [8]. By connecting together the gate to the body of a simple MOS transistor, the threshold voltage of the derived DTMOS is reduced upon forward biasing the body. This significantly increases the current drive of the DTMOS [29, 30]. However, a limitation arises with the significant reduction in the threshold voltage (V_t) of the MOS transistor due to standby power considerations in static circuits and possibility of failure in dynamic circuits which in turn leads to result in reduction of the gate overdrive and hence, the speed of working of the overall circuit. A remedy to this limitation can be achieved by contriving a dynamic

threshold MOS wherein, the V_t is low when the MOS turns on and vice versa. This exact behaviour is exhibited by a DTMOS by linking the gate to the body of a MOS transistor [29]. The reduced V_t of DTMOS is the result of reduction in the depletion charge which causes an increase in the inversion charge and hence higher current drive [31]. Figure 2 illustrates a simple n type DTMOS in which body terminal (B) is directly connected to the Gate terminal (G) of an NMOS. In a DTMOS, the bias voltage at the body terminal changes with input signal as per the relation in (1). This in turn dynamically changes the Vt of the transistor [32].

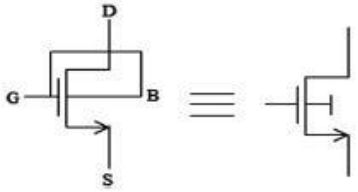

Figure 1 *MOS transistor using DTMOS*

$$V_{th} = V_{th0} + \lambda(\sqrt{|2\phi_B - V_{BS}|}) \quad (1)$$

where symbols have their usual meaning. In DTMOS technique, gate to source voltage VGS equals body to source voltage VBS and is equal to applied input voltage. Hence, VBS increases with increase in the input voltage while Vt decreases as per the relation in (1).

Small Signal Model of a DTMOS

In a DTMOS, the body terminal acts as a second gate which gives rise to a drain current component (Id) [33] given by

$$I_d = gmb.V_{BS} \quad (2)$$

where gmb is the body transconductance. The increment in I_d can be used to model gmb as

$$gmb = \frac{d\,I_d}{d\,V_{BS}} \quad (3)$$

Since Id depends V_{SB} on through the dependence of V_t on V_{SB}, it can be obtained

$$g_{mb} = \chi g_m \quad (4)$$

Where

$$\chi = \frac{\partial V_t}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2\phi_B + V_{SB}}} \quad (5)$$

The value of χ falls in the range of 0.1–0.3. This dependent current source is included in the small signal model of conventional MOS as represented in the Fig. 2 to came up with the small signal model of a DTMOS. Since body and gate are connected together in DTMOS, hence they can be a common terminal as shown in the Fig. 2. This body bias technique has several advantages over other low voltage techniques namely, high transconductance gain, larger bandwidth etc. As rise time is inversely proportional to bandwidth, hence this technique results in lower delay i.e., faster circuit operation [34].

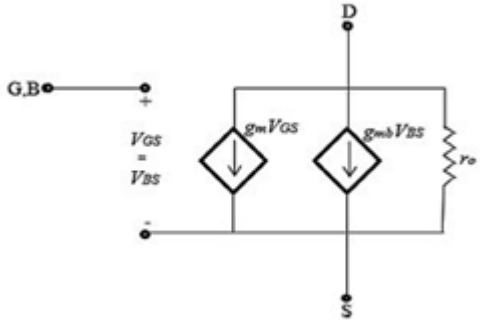

Figure 3 *small signal model of DTMOS*

IV. Proposed Current Comparator

Proposed Current comparator is shown in the figure.

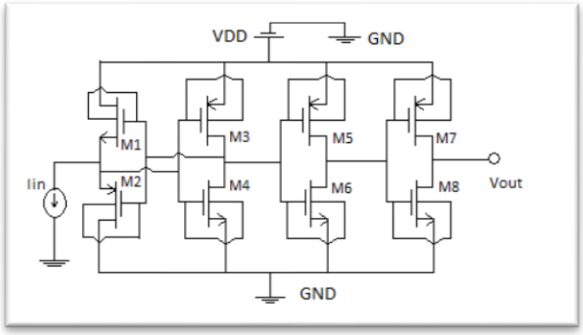

Figure 2 *Proposed Current Comparator using DTMOS*

Working Principle:- M1 **(**NMOS) and M2 (PMOS) act as AB class amplifier to amplify small current difference at input. It also gives the ability of applying feedback to the gates. **CMOS** inverter is used to achieve sufficient gain for amplifying small voltage variations at the input stage node. Back to back CMOS invertors are used to achieve rail to rail slewing.

V. Simulation and Results

The functionality of the proposed circuit is verified through LTSPICE simulations. The power supply of ±0.3 V is used .The DC and Transient response results are illustrated in the Figs. 5 and 6. Figure 5 shows the DC analysis of the circuit for input current I_{in} in the range of ±0.5uA. As can be seen that when Iin < 0, the output voltage of the current comparator is −0.3 V, switching occurs at the point where Iin = 0 after which the output voltage rises to 0.3 V, thus verifying the operation of the circuit. Figure 6 illustrates the DC gain of the proposed current comparator. Iin is varied from −10μA to 10μA in steps of 0.1μA. It can respond at low current as 0.5μA.

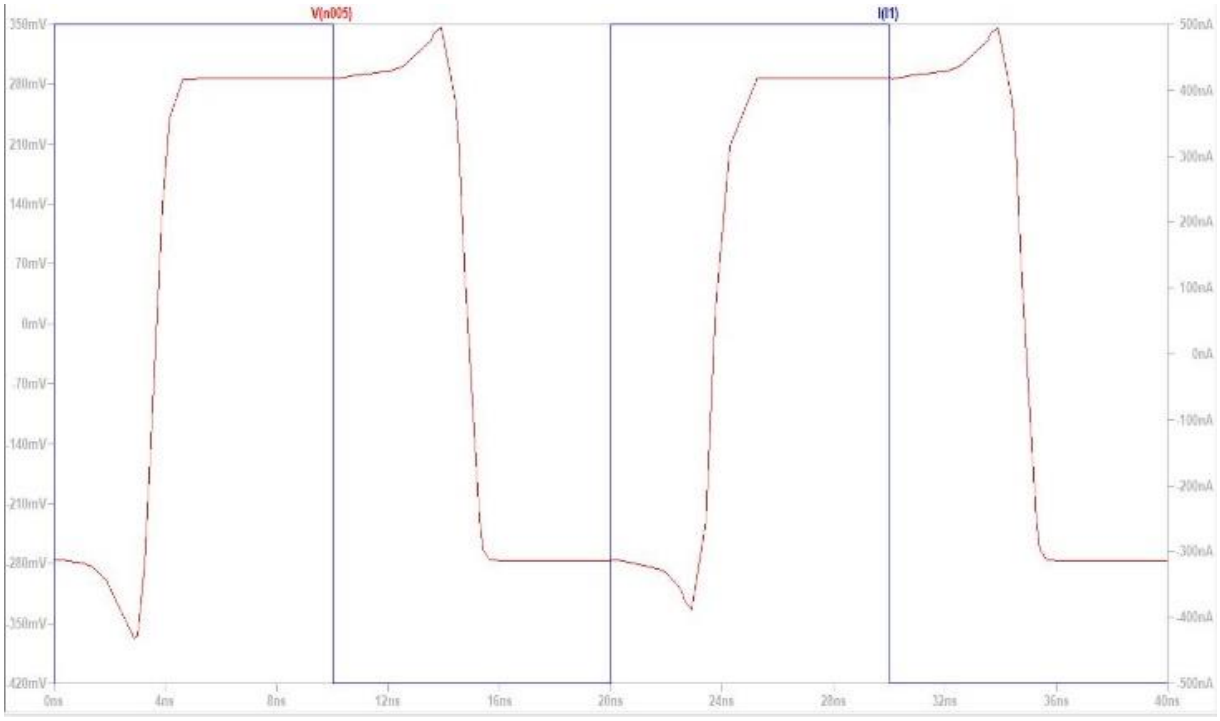

Figure 5 *Transient response of proposed comparator*

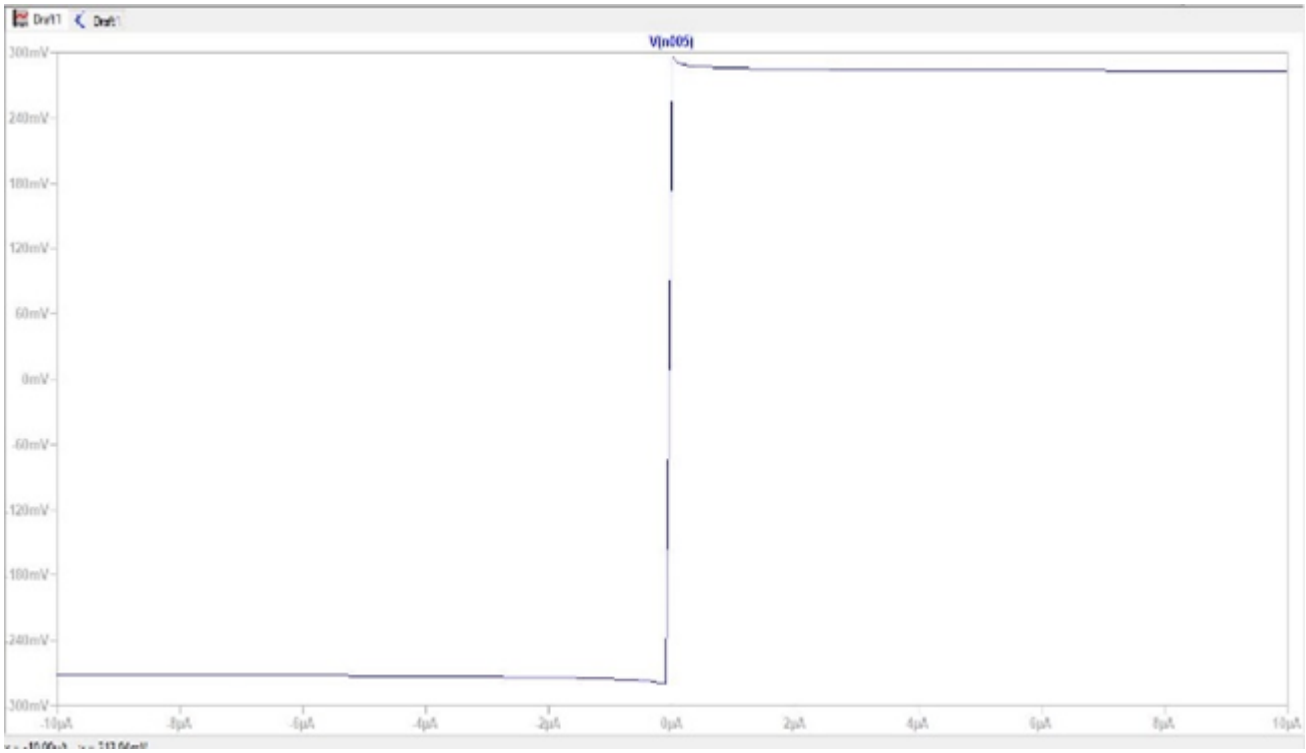

Figure 6 *DC response from proposed comparator*

VI. Bibloigraphy

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