Design of RAM using Quantum Cellular Automata (QCA) Designer

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Abstract: Quantum-dot cell automata (QCA) development as an alternative rather than Complementary MOS advancement on the nanoscale has a promising future; QCA is a captivating development for structure memory. The proposed structure and amusement of another memory cell structure subject to QCA with a base deferral, region, and multifaceted nature is shown to execute a static arbitrary access memory (RAM). This paper demonstrates the arrangement and propagation of a RAM with another structure in QCA. Since QCA is a pipeline, this RAM has a high working pace. It has the limit of a standard high working rate RAM that can give read/write actions as regularly as conceivable with least postponement. Decoders and multiplexers (MUXs) in QCA are shown that have been organized with a base number of larger part entryways and cells. The new RAM, decoders, and MUXs are arranged, completed, and replicated in QCA using a banner dissemination framework to avoid the coplanar issue of convergence wires. The QCA-based RAM cell was differentiated and the RAM cell reliant on CMOS. Results exhibit that the proposed RAM is progressively gainful to the extent region, difficulty, clock recurrence, and power use.

Index Terms: Quantum Dot Cellular Automata, QCA Wire, Majority Gate, Mux, Decoder.

I. INTRODUCTION

CMOS is an innovation, which has altered the universe of devices. Created more than forty years ago, the devices today has contracted to numerous requests of size. It is this scaling down that has brought about a proceeded with advancement as far as cost, execution and vitality productivity. Various reasons add to making CMOS the current best for microelectronics. Some of which incorporate the better conceivable adaptability, current reliance on channel width rather than producer territory, and low power utilization. Quantum-dot cell automata (QCA) have diverse Nano-level enlisting innovation [1]. The steady states of zero or one can be addressed by two. Stable plan of two or three electrons, which can include four spots corner to corner. The circuits executed using such gadgets does not require standard interconnections. Furthermore, have incredibly low power dissemination. The QCA cells, just as the circuits utilizing these cells, have been totally produced and attempted by various researchers [2-4]. Moreover; expansive research has been performed towards use of QCA relies upon the nuclear structures, which can work at room temperature [5-7]. The quantum dot cell automata use a matched portrayal of information, by dislodging the present switch with a cell having a bistable charge arrangement. One arrangement of charge addresses a combined "1", the other a "0", anyway no present streams into or out of the cell. The field from the charge arrangement of one cell modifies the charge game plan of the accompanying cell. Shockingly, this crucial apparatus joint effort is sufficient to help comprehensively valuable enlisting with low power dissemination. The basic element of a QCA cell is that it has an electric quadrupole, which has two stable Introductions as found in Fig. 1. These two introductions are utilized to speak to the two-paired digits, "1" and "0". A. QCA cell is a structure include four quantum-dots organized in a square pattern. QCA data preparing depends on the Coulomb repulsion between numerous indistinguishable QCA cells. The cells contain two different electrons, which repulse each other because of their common Coulomb repulsion and, in the ground state, have a tendency to involve the corner-to-corner locales of the cell. These prompt two polarizations of a QCA cell, meant as P=+1 and P=-1 separately. Hence polarization 0 and polarization 1 are encoded in polarization P=+1 and P=-1 separately. At the point when a second cell is set close to the primary cell, the Coulomb repulsion between the cells executes the decadence and decides the ground condition of the first cell [8].

Fig. 1(a) P=-1 (Binary 0), (b) P= +1 (Binary 1)

The paired wire exchanges the condition of the information cell to the yield, which frames the center idea in computerized planning i.e. exchanging contribution to yield. The idea of the wire is the coulomb’s law because of which the electrons of the contiguous cells are organized by the information cell with the end goal to stay away from shock because of electrostatic powers in fig 2. For instance if the information cell has a polarization of 1.00, i.e. it is basis 0 then the adjoining cells pursue a similar arrangement to accomplish the condition of most extreme steadiness. The execution of parallel wire is done on QCA designer tool programming apparatus and redress results have been gotten which are appeared in the re-enactment waveform [9].

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II. QCA BACKGROUND:

The structures (building hinder) that have been examined until now are altogether no concurrent structures and information is the main wellspring of vitality subsequently no power over exchanging. At the point when the information is connected to the variety of QCA cells, the fundamental component includes the difference in the condition of cells from ground state to left state. This cluster is relied upon to sink into another ground state. Anyway, without clock, the cells may have a progress to another metastable state, which may result in a flighty activity. The timing of QCA cells can overwhelm this. The timing is fundamentally for the control of hindrances between the cells, which thusly controls the exchange of electrons. The QCA timing plan comprises of four stages switch stage, hold stage, discharge stage and the loosen up stage. The stages are appeared in Fig.3 (a) Four checking zones are utilized in QCA. The cells are arranged in zones to such an extent that the field continue as before in every one of the cells in the zone. The idea lies in the range of impact of every electron can have the impact of it energize to a specific range. It is the technique for timing that makes QCA not quite the same as CMOS devices [10].

III. MAJORITY GATE IN QCA:

Majority function (sometimes quorum function) is a threshold function that produces a one if and only if the majority of the inputs are one. Otherwise, the output is 0. This function is only defined for three or more odd inputs. The majority function can be found in various applications such as adders, subtractors. In QCA, there are different types of majority gates are like three input majority gate and five input majority gate and 7 input majority gate used for the different application circuits. Here majorly using the three and five input majority gates for the circuits to design very optimizing. For the three input majority gate there will be having the three inputs and one output. In the three input majority gate if the major value is 0 then the output will be 0, similarly if the major value is 1 then the output will be 1. Similarly, it will be applicable to the five input majority gate. The symbols are represented in the fig 5(a) three input majority gate and 5(b) input majority gate [12].

There are two types of crossovers in QCA as shown in Fig 4(a) and (b) [11].
IV. INVERTER USING QCA:

Inverter is also known as the Not Gate. QCA inverter or NOT gate, when the information is having one consequently it gives the outcomes as 0. In addition, additionally when input is 0, at that point naturally output is 1. The outline is appeared in the fig (8). Here one of the input is y, which passes the incentive to central cell, and it inclines to some polarizing.

V. MULTIPLEXER:

Multiplexer is an essential component in numerous variation circuit plans, for example, the usage of a FPGA and memory circuits. This paper explores the executions of a 2:1 multiplexer in QCA and proposes a novel and productive plan. The proposed multiplexer has been contrasted with two recent plans as area, speed and delay. Examination of results describes the upgrades in our structure when contrasted with other methodologies. Additionally, Simulations explain that the proposed multiplexer is totally powerful to high information recurrence in contrast with its partners A 4-to-1 multiplexer consists four data input lines as D0 to D3, two select lines as S0 and S1 and a single output line Y. The select lines S1 and S2 select one of the four input lines to connect the output line. The particular input combination on select lines selects one of input (D0 through D3) to the output. The figure below shows the block diagram of a 4-to-1 multiplexer in which the multiplexer decodes the input through select line. The structure of 2:1 mux is and 4:1 mux is shown below fig (9) (a) and (b) [13].

VI. DECODER:

A decoder is a numerous information, various output logic circuit that changes codes input into coded output, where both the sources of input and output are disparate for example n-to-2n, and paired coded decimal decoders. Interpreting is basic in applications like information multiplexing, memory address translating, and 7 fragment display. The best case of decoder circuit would be an AND-gate since when every one of its sources of input are high, the output of this gate is High which classified dynamic High output is as an option to AND gate, the NAND logic gate is associated the output will be Low (0) just when every one of its sources of input are "High". Such output is designated dynamic low output.

A slightly more difficult decoder would be the n-to-2n type binary decoders. These kinds of decoders are combinational circuits that modify binary information from n-coded inputs to a most of 2n exclusive outputs. In case then-bit coded data has idle bit combinations, the decoder may have less than 2n outputs. 2-to-4, 3-to-8 line decoder or 4-to-16 decoder are other examples. The basic 2 to 4 decoder logic circuit diagram is shown in fig 10. The parallel binary number is an input to a decoder, used to notice the occurrence of a particular binary number at the input. The output shows existence or nonexistence of precise number at the decoder input [14].
VIII. PROPOSED MAJORITY GATE:
In the proposed majority gate 5 input majority gate is designed for the RAM cell for the performing the circuit optimizing the cell to get the required output information. Here this majority gate gave the major support for the designing the RAM cell and the 3 input majority gate is also used to design the circuit. The proposed majority gate is shown below in fig 11.

![Fig.11 proposed majority gate](image)

7.2. PROPOSED 2X1 AND 4X1 MULTIPLEXER USING QCA:
In general, an electronic multiplexer makes it possible for several signals to share one expensive device or other resource, for example one A/D converter or one communication line, instead of having one device per input signal. As a result, the multiplexer is an extremely important part of signal control systems, because it allows the system to choose one of several inputs to be forwarded to one output. The selection bus determines which input signal is allowed to pass through to the output unchanged. In this paper, we present the design and simulation of QCA 2 to one multiplexer in order to explore design methods for designing 2n to 1 multiplexers. The design of the 2:1 mux and 4:1 mux circuit diagram of QCA are shown in fig 13(a) and (b).

![Fig 13(a) 2:1 mux   (b) 4:1mux](image)

For designing the 2:1 mux in QCA it consists of the one AND gate and the one OR gate and it is the combination of the both the gates for 2:1 mux and 4:1 mux. However, for designing the 4:1 mux it is design by using the 2:1 mux and AND gate and OR gate. Clocking phases of the pairs are traversed in the proper order (0, 1, 2, 3, 0, 1,) so that the required clock phases are

Always presented at the proper sequence in order propagate the signals correctly and produce signal delay equal to the number of the included cell pairs. The reason for using two cells clocked to the same phase for every quarter of clock delay is to isolate the state of every pair from the state of the cell located next to the output of the delay block. Furthermore, it is well known that the design robustness depends on the non-uniformity of cell distribution in clocking zones. For example, if the clocking zones consist of a great number of cells the corresponding design can only operate in very low temperatures because of thermodynamic effects. In the presented design, the use of clocking zones with many cells is avoided and consequently the QCA cells are uniformly distributed into the clocking zone.

7.3. PROPOSED 2x4 DECODER USING QCA:
Computerized rationale circuits to get to the memory exhibit for example decoder circuits (2-to-4 decoder) in QCA. It is executed with the assistance of three information sources dominant part entryways, which is effective in all viewpoints in contrast with past 2-to-4 decoder plans in QCA. In Beginning, past plans of 2-to-4 decoder, which is as of now effectively actualized in QCA are exhibited and after that our structure is proposed in fig:13.

A fundamental 2-to-4 decoder circuit with enable input is used. The fundamental structure square of this decoder has one phase of 2-to-4 decoder which requires four 2-input AND gates, since absolute number of rationale mixes, that can be shaped with two factors is four. Each consistent mix of two factors A and B are given to information ports of separate AND doors. The supplement of every factor is taken by putting an inverter, just before the contributions of AND gates. In second phase of 2-to-4 decoder we requires four more AND entryways to perform intelligent AND activity of, first stage AND gates yield with Enable line input. The subsequent stage AND doors have the capacity to empower or cripple the decoder yield as indicated by intelligent estimation of empower input. In this way, it requires aggregate, eight AND gates to actualize a fundamental 2-to-4 decoder. This structure square can likewise be planned in QCA innovation with various greater part doors (three information sources MV and five data sources MV). Here every lion's share doors is utilized to perform intelligent activity in their separate stages. The reversal task of each information variable is performed by putting the cell corner to corner. The 2-to-4 decoder functions as pursues: If the contribution to the empower line (EN) is high (rationale '1'), it enacts the 2-to-4 decoder as ordinary activity while if the empower line (EN) input is low (rationale '0') it deactivates the decoder and confines all yields to wind up handicapped or rationale 0 is appeared in fig 14.
7.4. PROPOSED RANDOM ACCESS MEMORY:
RAM cell with Set / Reset ability, using 2 × 1 multiplexer. A Schematic of this multiplexer is shown in Fig. 14(a). In this schematic, if Select = ‘0’, then Output = ‘in0’, and if Select = ‘1’, then Output = ‘in1’. Also QCA layout of this multiplexer can be seen in Fig. 14(b). In this layout, three-input majority gates are used to design AND, OR gates. This design has good results in terms of output stability against temperature changes. A schematic of this RAM memory cell is shown in Fig. 15. In this structure, when Read / Write = ‘0’, regardless of the Set / Reset and Select values, output value will not change, and in this case, the value of cell can be read. And when Read / Write = ‘1’, and other Set / Reset and Select inputs are equal to zero, the output value is zero, in this mode clear operation of memory cell is done. Also if Read / Write = ‘1’, Set /Reset = ‘1’, Select = ’0’, then output =’0’, and Set operation of memory cell is done. Finally, if Read / Write = ‘1’, and select = ‘0’, regardless of the Set / Reset input value, new input value takes place in output and the write operations of cell is done. QCA layout of this RAM memory cell. In our simulations, this layout is more optimal than the memory cells layout by D-Latch and SR-Latch, in terms of number of QCA cells, occupied area and stability in output result.

VIII. RESULTS AND DISCUSSION
In the results and discussion showing the wave forms of the proposed majority gate and the 2:1 mux and 4:1 mux and the 2 to 4 decoder and proposed RAM cell in the fig 16(a),(b),(c),(d).
IX. CONCLUSION:
This paper presents the design and simulation of an 1 bit RAM in the QCA technology. The proposed RAM is a flexible and powerful structure using programmable logic and interconnections. The simulation results of all blocks of the proposed RAM used QCA designer In comparison with other studies, the presented memory cell acts as a pipeline that decreases delays and increases operating speed. Different applications can be defined using the proposed RAM. The designs can be implemented using the QCA Designer software tool and simulated by the QCA Designer. The results showed that the proposed RAM performs a task with the excellent efficiency. According to our paper all the blocks are simulated in the QCA designer and noted the values of area, number of cells used for the RAM cell.

REFERENCES: