Advanced Error Control Method For 3-D Noc

Ashok Kumar K, Vanga Karunakar Reddy

Abstract: Occurrence of errors is frequent in on-chip interconnects when technology is scaling down. The errors are majorly affect data bits thereby loosing performance or data bits in on-chip interconnecting links. To control the errors without affecting performance, an efficient error control method is required. From literature, a combined error control method are used which is controlled multiple errors efficiently in on-chip interconnects. 3-D NoC is the one of major intercommunications for SoC because of parallel processing. Controlling the faults in 3-D is quite complex comparatively than 2-D NoC hence proposing integrated method for controlling faults. The improved NoC design is presented 48% of performance than existing designs hence the improved 3-D NoC design exactly suitable for FPGA based SoC.

Keywords: NoC, Transient fault, Hamming code, CRC, FPGA

1 Introduction

Reducing chip size increases millions of components in on-chip of system on chip (SoC) tremendously which also increases sources of fault thereby decreasing the overall performance. Bus based communication is achieved the interconnection among the intellectual property cores (IP). With an advance of technology, number of IP cores increases continuously hence limiting performance in terms of latency, throughput and power consumption. To get compatible speed of chip multiprocessor (CMP), an efficient intercommunication protocol is required with less complexity. Bus based communication is the popular for SoC because of simple and easy however, it is compatible when number of devices are limited. When number of on-devices is large, intercommunication among devices is critical in terms of scalability and reliability. Network on chip (NoC) is the new paradigm of intercommunication for on-chip devices of SoC. Because of parallel structure; NoC is provided high performance in terms of scalability, flexiblity and reliability. The NoC is constructed of mainly three components that are routers, network interface and interconnects. Router is crucial component for NoC which is responsible of data packet transfer from input port to output port. As NoC supports parallel structure, the router is controlled multi-input and multi-output ports. The data packet is controlled at router which coming from any port of multi-input port to any one of multi-output port. To control data from multi-port, an efficient scheduling algorithm is required to improve speed of arbiter. a crossbar switch is used for data transfer from selected port to output port. Network interface (NI) is adapter between the router to processing element (PE). The PE is an either processor, memory or an I/O device. The data packets are started from PE and decoded at NI thereby passing through routers and finally reached to destination. The on-chip interconnects are also plays major role when transferring data packets from port to port. The number of on-chip interconnects are also affected the power consumption of overall NoC based SoC. Finally, NoC is a solution of intercommunication protocol for modern SoC that is information is transferred parallelly among PEs.

Still, the performance of NoC is affected with critical an issue like faults in interconnects, ageing and failure of routers. The faults are major concern in NoC based SoC because of data packet loss and reducing yield of system. To increase yield and reliability of NoC, fault tolerant methods are required. With use of fault tolerant techniques, the data packets are protected and also network errors like deadlock, livelock are avoided completely. The faults are not only affecting the performance of NoC but also damaging the hardware components of NoC like failing of routers and failing of PEs thereby affecting the hardware redundancy. Majorly, the faults are two types one group is soft faults which occurs and fade out instantly. Another type of group is permanent faults or hard faults which occurred and affected the data packet or hardware of NoC. Hence, an efficient fault tolerant method is required to control the faults and to obtain reliable communication between input port to output port of NoC. 2-D NoC is highly dominated structure for current SoC designs because of high performance and reliable communication. Because of wiring and layout constraints, the performance of 2-D NoC limited for various networks. However, the fundamental change for SoC is 3-D NoC in near future. Fig.1 depicts 3-D NoC structure that is improved from 2-D NoC based SoC. 2-D mesh based designs are connected with up and down interconnections which is required as router with extra connections that are up and down ports.
The conventional router of NoC has four directional ports for interconnecting neighbour routers and one local port for PE. The router of 3-D NoC is required two extra connections for interconnecting up and down routers hence requiring six ports for interconnection of neighbour router and one port for PE. One of the major advantage of 3-D NoC is stacked mesh which hybrid method between packed switched network and bus. It combines multiple layers of 2-D packet network with bus for entire chip thereby obtaining the advantage of both mesh topology and bus. Because of distance among layers of 2-D in 3-D NoC is small, overall length of bus is also very small comparatively hence compatible for z-axis of 3-D NoC based SoC. Another advantage of 3-D NoC is construction that is adding extra layers for PEs and also restricting to one layer for router. With these advantages, a 4x4x2 mesh based 3-D NoC is designed where each router has two PEs hence requiring total of eight ports per router. The proposed 3-D NoC shown reduced bandwidth and less connectivity however, energy consumption will reduce when it is simulated at specific traffic patterns.

2 Related Work
An advance in technology integrates millions of on-chip components in single integrated chip (IC) thereby increasing number of faults. The common approaches of fault tolerant are divided into two categories. First one adding hardware redundancy to NoC for controlling faults which needed extra logic to data. Cota et al. [1] surveyed on fault tolerant methods of error control codes (ECC), cyclic redundancy check (CRC), retransmission codes, spare wires and triple modular redundancy (TMR). Second one is adding of extra hardware to enable NoC for fault free path. The second category is less dependent comparatively than first category and also need less hardware. Rodrigo et al. [2] proposed the uLBDR algorithm which is the first version of fault tolerant method. LBDR is given condition of the neighbour routers and also associated routes that are available or blocked. If minimal path is not available, the LBDR is de-routed and tried for minimal path towards destination. Eghbal et al. [3] analyzed different factors that are affected reliability and also categorized different faults that are physical and logical faults. The failure analysis of through silicon via (TSV) is presented using formal method first thereafter mean time to failure (MTTF) is used for 3-D NoC router. An analytical model is also presented to present a report on probability of system failure that is TSV failure rate. However, the proposed model is time consuming. Pano et.al [4] proposed a workload-aware routing technique by complementing the existing algorithms thereby optimizing the traffic of network. To improve the router and port utilization in network, the priority based routing and workload signature is utilized in proposed methodology. The network utilization and latency are improved when compared with baseline, XY, west-first and north-last algorithms. However, the improvement of proposed work is presented when number of hops is limited and the proposed work is suitable for 3-D NoC. Vivet et al. [5] are presented 3-D scalable and modular NoC architecture by using asynchronous logic. It is made up of two die layers thereby integrating ESD protection and design for testing with fault tolerant scheme. The proposed 3-D NoC links are obtained better energy consumption and data rate than existing work because of parallel NoC links. Vivet et al. [5] concluded that the 3-D NoC is provided efficient energy, high bandwidth and low latency when compared with 2-D NoC. Wachter, E et al. [6] are proposed an integrated approach with previous recovery approaches thereby tolerating severe faults. A hierarchical and distributed fault controlling mechanism is presented that is fault notification hence recovering process for fault and also combining path discovery to enable fault tolerance in high defective system. By combining both NoC fault recovering mechanisms of transient and permanent faults, the integrated approach is tolerated severe faults thereby operating faults in degraded mode or fault-free path. The recovered time of proposed approach is small when compared with other fault tolerant mechanisms. However, the integrated approach is suitable for 2-D NoC systems. Hence, there is a huge scope research on fault tolerant mechanism in 3-D NoC systems. This paper is proposed a novel approach for controlling of both transient and permanent faults in 3-D NoC. The fault notification mechanism is used to fault recovery in path discover network that is consisted of data packet is divided into number of flits. The improved method is simulated and synthesized in Xilinx thereby analyzing performance of 3-D NoC in FPGA target device.

3 Fault Notification Method
A defective component of system is produced wrong results thereby leading the system into failure. The faulty hardware is given improper output for entire system. Hence, there is a need to isolate the fault from faulty module and also avoid the propagation of fault to remaining system. Network Interface (NI) is embedded fault control method to avoid propagation of faults to the other parts of system. Most of the fault control mechanisms are required extra hardware in NI thereby increasing area and reducing speed of the NoC router. Hence, this paper is proposed an improved fault control mechanism for NoC based SoC. The proposed 3-D NoC is composed with extra circuit for controlling faults at data transfer in NoC interconnection links. The extra components of cyclic redundancy check (CRC) and exclusive-or gate embedded in both transmit and receive NI for identifying fault in interconnection link. Fig.2 presented
the recovery method for transient faults after detection and correction. The CRC coder and decoder are verified the outgoing and incoming data packets from input and output buffer.

![Diagram of test and test recovery modules for controlling of transient faults](image)

**Fig.2 Test and test recovery modules for controlling of transient faults**

This verification is enabled to identify the faults in components of router and also interconnection links. Whenever the fault is detected in data packet, CRC coder stops the data packet transfer thereby isolating particular circuit from data transfer and also notifying to adjacent router. Whenever adjacent router receives fault notification, the neighbour router will check the both interconnection links [7]. If the interconnection channel is fault-free, neighbour router is requested to re-send the data packet from source to destination. If the interconnection link is not fault-free, test pattern generator and test response analyzer modules are enabled to identify the fault type [8]. Each NI has both TDM and TRA to check the healthy status of interconnection link thereby avoiding propagating fault to remaining parts of module. The test module is worked as same as BIST for combinational circuits because of simple and easy to implement to any design.

### 4 Results and Discussion

An improved architecture of 3-D NoC router is simulated and synthesized in Xilinx 14.7 ISE software and verilog HDL is used for behavioral simulation. The implementation results are analyzed in terms of area utilization, delay and power consumption in Vertex-6 FPGA target device.

![RTL schematic of improved NoC router architecture](image)

**Fig.3 RTL schematic of improved NoC router architecture**

Fig.3 presented RTL schematic view for improved 3-D NoC router that is eight input and output ports. Eight input and output ports are connected to the crossbar switch that is transferred the data from selected port to the output port. The DRRA is selected high priority input port to data transfer thereby avoiding arbitration among ports. The directional ports and local port are used to transfer the data from source PE to destination PE through the crossbar switch. As 3-D NoC is used to transfer data between ports, performance is increased when compared with 2-D NoC. Fig.4 described the performance of 3-D NoC router in terms of area utilization, delay and power consumption. The area utilization is presented in terms of Slice LUTs, Slice registers, LUT-FF pairs and bonded IOBs. From Fig. 4(a), it is clear that the improved NoC design is occupied less area in target FPGA device because the improved 3-D NoC design is required simple circuit to recover faults. Fig.4 (b) showed power consumption of 3-D NoC circuit in terms of static and dynamic. From ITRS, it is known as the static power consumption is impacted more than dynamic power consumption after 14nm of CMOS circuits.
2.3. Power Supply Summary

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<th>Power Supply Summary</th>
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<tr>
<td>Total</td>
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<td>Supply Power (mW)</td>
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Fig. 4 (a–c) Synthesis results of improved 3-D NoC router in terms of area utilization, delay and power consumption

From Fig. 4(b), it is inferred that the dynamic power consumption very less than static power consumption because of less number of transitions for fault recovery. Fig. 4(c) presented speed of the proposed NoC router in terms delay and maximum frequency. The minimum period between clock cycles is 1.890ns which is very low for NoC based SoC. From Fig. 4(c), it is clear that the speed of proposed NoC router high for FPGA based SoC design. Table 1 shows comparison of proposed 3-D NoC design with existing designs.

**Table 1 Performance comparison of Baseline [9], FT PE [6] with proposed design**

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<td>Area Utilization</td>
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<tr>
<td>Slice Registers</td>
<td>1709</td>
<td>2933</td>
<td>402</td>
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<tr>
<td>LUT-FF pairs</td>
<td>827</td>
<td>840</td>
<td>236</td>
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<tr>
<td>Bonded IOBs</td>
<td>258</td>
<td>422</td>
<td>118</td>
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<tr>
<td>Delay (ns)</td>
<td>4.25</td>
<td>2.672</td>
<td>1.809</td>
</tr>
<tr>
<td>Dynamic Power consumption (mW)</td>
<td>15.69</td>
<td>11.23</td>
<td>9.86</td>
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From Table 1, it is cleared that the proposed design is increased approximately 48% of speed and 15% of dynamic power consumption than FT PE [6]. The area utilization is also improved massively when compared with Baseline [7] and FT PE [6] because of 3-D structure and also improved fault recovery method. Hence, the proposed design is showed higher performance and higher reliable communication than existing NoC design. This paper is majorly concentrated on power consumption because of 3-D NoC is dissipated power with increasing of temperature.

5 Conclusion

Power consumption is majorly important in VLSI based digital circuits because of dynamic transitions when data is transferred. NoC is the acceptable solution for FPGA based SoC designs because parallel communication between source and destination. Still, power dissipation is important aspect for NoC based SoC because addition of circuits for NoC to control faults and also recover. This paper is proposed an improved solution for fault control in 3-D NoC designs. The CRC based fault notification mechanism is used to identify faults and recover fault if it is detected. The improved NoC design is simulated and synthesized to identify the performance thereby proving the proposed mechanism is better when compared with existing designs.

References


