Abstract:— A voltage source inverter is commonly used to supply a variable frequency variable voltage to a three phase induction motor in a variable speed application. The output voltage contains harmonics, the different types of harmonic elimination methods are available. But all the methods having some limitations (both magnitude of harmonics and design of filters). This project deals with how to reduce the particular harmonics in the output voltage of inverter. The concept of multilevel voltage source inverters and their modulation topologies are to be analyzed. The concept of the Harmonic Stepped-Waveform technique for a multilevel inverter is to be presented. By applying this concept, specific harmonics can be eliminated, and the output voltage THD can be improved. A procedure to achieve the appropriate switching angles are to be proposed. A cascaded H-bridge multilevel inverter that can be implemented using only a single dc power source with only eight power switches and capacitors. Standard cascaded multilevel inverters require n dc sources for 2n + 1 levels. Without requiring transformers, the scheme proposed here allows the use of a single dc power source (e.g., a battery or a fuel cell stack) with the remaining n – 1 dc sources being capacitors, which is referred to as hybrid cascaded H-bridge multilevel inverter (HCMLI). It is shown that the inverter can simultaneously maintain the dc voltage level of the capacitors and choose a fundamental frequency switching pattern to produce a nearly sinusoidal output. This paper mainly focus on control of seven-level HCMLI with fundamental frequency switching control and how its modulation index range can be extended for reducing desired lower order harmonics. The proposed project are to be simulated by using MATLAB and the results are to be compared with experimental setup. The embedded controller is to be used for generating required pulses to the cascaded multi level inverter.

Index Terms:— Optimization, signals, harmonics, ANT colony, multilevel inverter voltage and current.

1 INTRODUCTION
Nowadays the direct drive wind energy conversion system is very much attractive because it has lot of advantages such as no need of gear box, low maintenance, nose less operation operating at maximum power point region. But it requires the full scale power converters for regulating the voltages and frequencies based on grid requirements. The wind power generation is fluctuating with respect to time to time due to stochastic nature of wind speed. Hence the stability becomes very sensitive during grid conditions. Among various types of low speed wind generators the PMG appears to be more promising. The cost of permanent magnet has declined significantly in recent years making it practical and cost-effective and has the advantages of higher efficiency, high energy yield and better reliability. The PMG allows larger number of poles in its construction with small pole pitch and yields cost effective design. Nowadays lot of power conditioning circuits is addressed in the literatures such as voltage source inverter, current source inverter, quasi resonant inverter, neutral clamped inverters, quasi Z-source inverters etc. Recently the multi level inverter is very attractive solution for power quality improvement in grid connected WECS. The multi level inverters are mainly utilised to produce stair case waveforms and also used to regulate the desired voltage and frequency of generated voltages.

The fluctuating voltages and frequency if generator is feed to full scale power converters such as rectifier and MLI as shown in Fig. 1. The MLI provides the desired voltages and frequency that is controlled by the modulation index from the control block.

2. CASCADED MULTILEVEL INVERTER
The capacitors are used as the DC sources. The DC source for the first H-bridge (H_1) is a battery or fuel cell with an output voltage of V_{dc}, while the dc source for the second H-bridge (H_2) is a capacitor whose voltage is to be held at V_c. The output voltage of the first H-bridge is denoted by v_1 and the output of the second H-bridge is denoted by v_2 so that the output voltage of the cascaded multilevel inverter is

2.1. Modes of Operation
Figure 5.1 shows the circuit diagram of cascaded multilevel inverter. This cascaded MLI generated seven levels staircase wave form at which reactive power can be injected. It consists of two capacitors with different voltage level such as V_{dc} and 2V_{dc}.

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Based on the voltage injection and commands for the controller, the switching states are varied. By proper switching of IGBT’s in MLI can produce staircase voltages. This MLI consists of operating modes in one half cycle. Table 5.1 shows the switching sequence of MLI.

### Table 5.1 Switching sequence of MLI

<table>
<thead>
<tr>
<th>Load Voltage</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>S6</th>
<th>S7</th>
<th>S8</th>
</tr>
</thead>
<tbody>
<tr>
<td>+3V&lt;sub&gt;dc&lt;/sub&gt;</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>+2V&lt;sub&gt;dc&lt;/sub&gt;</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>+V&lt;sub&gt;dc&lt;/sub&gt;</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>-V&lt;sub&gt;dc&lt;/sub&gt;</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>-2V&lt;sub&gt;dc&lt;/sub&gt;</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>-3V&lt;sub&gt;dc&lt;/sub&gt;</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
</tbody>
</table>

**Mode 1:**
During this mode the switches S1 and S2 are conducts and produce a voltage level of +V<sub>dc</sub> as shown in Figure 2.

**Mode 2:**
In this mode the power switches S5 and S6 are conducts and 2V<sub>dc</sub> voltages are appears across the load as given in Figure 3.

**Mode 3:**
In this mode the power switches S1, S2, S5 and S6 are conducting and the terminal voltage 3V<sub>dc</sub> are appears in the output terminal as shown in Figure 4.

**Mode 3:**
To reduce the level in the staircase 3V<sub>dc</sub> to 2V<sub>dc</sub> the switches S1 and S2 are turned off and maintain the S5 and S6 ON state. Similarly, to reduce the voltage level from 2V<sub>dc</sub> to V<sub>dc</sub> switches s5 and s6 turned OFF and again S1 and S2 tuned ON. Similarly, the switches S3, S4, S7 and S8 are operating for getting the seven level negative staircase wave forms.
3. PULSE WIDTH MODULATION TECHNIQUES

Multi carrier phase disposition modulation technique has to be used to control the proposed MLI topology. This strategy is used to achieve the lowest harmonics in voltages. In this method carriers are same in frequency, amplitude and phase. The reference waveform has peak to peak amplitude $A_M$, a frequency $f_m$, and its zero is centered in the middle of the carrier set. The reference signal is compared with each of the carrier waves. If the reference signal is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off.

![Reference wave Carrier wave](image1)

**Figure 5.7 Phase Disposition Modulation**

Next, a critical evaluation of the aforementioned PWM schemes on the basis of application for single and three-phase inverters is provided, thereby providing the framework and guidelines for the selection of the appropriate technique for each application area. Evaluation criteria include harmonic loss factor and total harmonic distortion factors defined at the input and output of the inverter terminals. Finally, a simple low-cost solution for obtaining the required PWM switching points is proposed.

4. RESULTS AND DISCUSSIONS

The experimental photograph of cascaded MLI is given in Figure 5.12. The experimental setup consists of eight IGBT power switches, driver circuit, isolation circuit and control circuit. The FPGA SPARTON.6 processor operating at 20 MHZ is used to realize and control the performance of MLI based STATCOM.

![Figure 5.12 Experimental setup of Proposed Cascaded MLI](image2)

For the control of MLI and to compensate the reactive power at which voltage sag occurs, the pulse width modulation is suggested as shown in Figure 5.13. The corresponding line voltages of MLI are depicted in Figure 5.14. Based on the voltage injection and reactive power management of the MLI, the PWM pulses are varied from Figure 5.15 these observed that the MLI produces stepped wave form which is almost sinusoidal and hence the THD injection to the grid is very minimum as shown in Figure 5.16.

![Figure 5.13 Experimental pulse pattern of Cascaded MLI](image3)

![Figure 5.14 Experimental Voltage and current THD spectra of Cascaded MLI](image4)

![Figure 5.15 Experimental phase Voltage and current waveform of MLI](image5)
5. CONCLUSION
The harmonic optimisation of stepped square wave signal produced by the multilevel inverter is analysed. The harmonic level and lower values of harmonics are mitigated by using ANT colony optimisation techniques. The multilevel inverter is presented and analyzed in detail for different values of input voltage and frequency. It is observed that it can be implemented by using different switching strategies at which order of harmonics are analysed to validate the optimisation results.

REFERENCES