Design Of Software Defined Based Receiver(SRR):A Review

Bharat Naresh Bansal

Abstract: The wireless industries are growing exponentially with the development of multifunctional, multi mode communication standards and new radio access technologies. Software Defined Radio (SDR)[5],[6] technology is expected to replace several conventional techniques to implement transmitter and receiver, which offers extensive advantages that includes adaptability, multifunctionality and reconfigurability encompassing radio frequency bands, waveforms, modes of operation and air interface etc..So, Software defined radio becomes a vital technique for wireless communication in current era. This paper is based on review of various study related to design techniques of SDR or SRR. It contains brief introduction of SDR, advantages, SRR basic components and also discuss the observations based on various design techniques.

Index Terms: Coefficient, Channelizers,Channel bandwidth,Computational complexity, FIR(Finite Impulse Response) filter,Power consumption, Reconfigurable, SDR or SRR.

1. INTRODUCTION

1.1 SOFTWARE DEFINED RADIO (SDR)

Joe Mitola[1][2] has introduced the concept of SDR which is included in the group of reconfigurable orre-programmable radios. Its characteristics are defined by software with dynamic capabilities.In SDR, software modules are utilized to create radio functions related to signal generation at transmissionend and signal reception at receiver end. In other words, SDR is a radio that offers flexibility in static hardware by the use of software. Therefore, the same part of hardware may be employed to performvarious tasks at different points of time[3],[4],[5]. The characteristics along with advantages and disadvantages of SDR are explained in section 1.1.1 and 1.1.2 followed by Software Radio Receiver and its applications.

1.1.1 CHARACTERISTICS OF SDR

SDR has following characteristics[6]:

a)Multifunctionality: Software defined radio support different types of services or communication standards due to its reconfiguration property. With the development of short-range networks i.e. IEEE 802.11 or Bluetooth, there is enhancement in the services of radio.

b) Global mobility: The 3G technology is used and it can be synchronized with various standards such as 1G, 2G, 3G and 4G. There are many standards under this3G umbrella; therefore, the requirement of transparency is sorted out using software radio concept.

c) Compactness and power efficiency: A compact and power efficient communication system is implemented using software radio approach. This factor is useful especially in cases, where there is enhancement in the number of systems because the same piece of hardware is repeatedly used to implement variety of systems and their interfaces.

d) Easiness in manufacturing and upgradtion: Here a number of standard are clubbed in the same zone, therefore, it becomes very easy to manufacture and upgrade the system. A system can be easily improved and updated with additional functions due to its flexible design. It can be achieved efficiently without any cost to recall all the involved units or replace the user terminals.

The radio spectrum in SDR is dynamically explored and the portion of frequency band is determined. Hence, objective of SDR is to implement different types of communication medium on a general purpose hardware platform which is reconfigurable. Moreover, different types of modulation and demodulation techniques in wide and narrowband process are controlled by developing standards over a broad frequency range using software.The SDR has following types of levels7 (as per table 1):

- *Dr. Bharat Nareseh Bansal is working as Incharge and Associate Professor in the department of Electronics and Communication Engineeringat MIMIT, Malout, Punjab, India. He received his B.Tech. from Amaravati University, M.Tech. from PTU, Jalandhar and PhD from IKGPTU, Jalandhar. He has 13 years of work experience. He has to his credita round 22 research papers in journals and conferences. His areas of interest are Communication & Instrumentation. He is a life member of various technical associations.*
- *E-mail: bharat.mimit@gmail.com*

Table 1: *Various Level of SDR*

Levels	Name	Description
Level0	Hardware Radio(HR)	Design using hardware components and cannot be used
Level1	Software Controlled Radio(SDR)	Software used to implement control functions such as interconnects and power levels
Level2	Software Defined Radio(SDR)	It is software approach which control various security related function, wideband or narrowband process and modulation technique in communication system
Level3	Ideal Software Radio(ISR)	The whole system is controlled by programs with analog conversion only at antenna
Level4	Ultimate Software radio(USR)	Defined for comparison purposes only

1.1.2 Advantages & Disadvantages of SDR

SDR offers the following advantagess over traditional fixed radios:

a) A common set of hardware is used for reception and transmission of signals by using various modulations and encoding techniques.
b) There is a possibility to choose an operating frequency and mode which is best suited for prevailing situations.
c) User can modify or update the performance of a system by installing new software.
d) SDR provides an opportunity to identify interference of the system with other communications channels and also helps to avoid any interference.
e) It simplifies and improves the performance of radio architecture by eliminating hardware and its costs.
f) It provides a platform for carrying out latest experiments.

SDR has following disadvantages[5]:

a) It includes poor dynamic range in comparison to fixed radios.
b) It is not user friendly for writing and maintaining various softwares for different communication systems.

1.1.3 Software Radio Receiver (SRR)

The receiver which is used in SDR is known as SDR receiver or SRR. SRR requires real time variable frequency response characteristics, which are defined by software. Channelizer is the most intensive computational part of SRR that operates at sampling rate which is quite high. This process of extracting various narrowband radio signals from a wideband input signal in SRR is known as channelization. The filters that are used for channelization are called channel filters. Channel filter used in SRRs should have low complexity and reconfigurability property. The bandwidth of the filter is the important characteristic in radio receiver that selects the desired channel. Desired channel is selected using sharp filters having different bandwidths in SRR. The large number of filter coefficients and different computational resources are its major requirements. So, SDR receiver or SRR can receive channels of wide range of bandwidth and any modulation.

Figure 1 represents the basic functional diagram of SRR9. The receiver starts with smart antenna which is used to minimize different type of noise, multipath and interference by providing gain versus direction characteristic. Similar advantages are also provided by the smart antenna to the transmitter.

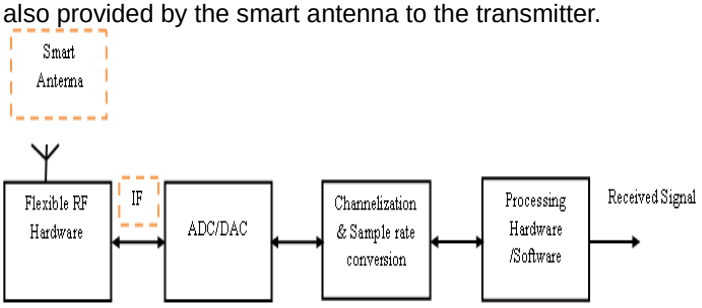

Figure 1. *Basic functional diagram of SRR*

In conventional SRR, low noise amplifier (LNA) is used for amplifying and filtering the radio frequency (RF) signal received by antenna, which after mixing with local oscillator (LO) produces an Intermediate frequency (IF). The IF range signal is digitized using analog to digital converter (ADC),It also eliminates imaging or carrier offset problems. Digital to analog converter (DAC) is used for converting digital signal to analog signal for transmitter. In the next stage, digital filtering is used for channelization process. Interfacing between the output of ADC and processing hardware is achieved using sample rate conversion. Different types of platforms are used for software processing like Digital Signal Processing(DSPs), Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs). The different type of software methods have been used for modulation and demodulation of the signal such as middleware or virtual radio machines.

1.1.4 Applications of SRR

Following are the applications of SRR:

a) SRR used in military as the Joint Tactical Radio System.
b) SRR is equally usefulfor commercial purposes. The commercial sector perceives SRR as a system that can implement in a particular range of capabilities, which are reconfigurable with the help of software.
c) It is securely upgradable which can be used in internet as medium for updates.

2. Software Radio Receiver (SRR)

Zangi and Koilpillai (1998)[9] presented an algorithm for implementing computationally efficient FB channelizerfor extractingparticular channels from the output of the wide-band ADC. The input of IF processing block is the output of the ADC in SRR.The IF processing block in SRR is implemented by using the computationally efficient algorithm. In this algorithm instead of classical DFTFB channelizer a subsampled DFTFB channelizer was used. The implemented channelizer had considerably less complexity than the traditional channelizers. Fixed channel stacking is major drawback of DFTFBs. Seskar and Mandayam (1999)[10] presented a reconfigurable architecture for linear multiuser detection. SRR was implemented to achieve dynamic reconfiguration. Authorshave

divided the functionality of the architecture into two parts according to processing speed requirements that is FPGA and DSP. The architecture has provided diverse Quality of Service (QoS) guarantees ranging in several orders of magnitudes in terms of Bit Error Rate (BER) requirements. As the architecture was flexible, therefore it allows different signal processing approaches for the implementation of required estimation. Moreover, the experimental results showed that diverse services such as voice and data traffic were simultaneously supported using this architecture. There was degradation in receiver performance due to fixed point arithmetic, which was compensated by 4-bit quantization. Zangi and Koilpillai(1999)[11]describedtwo key issues in the design of wideband SRR which are: a) a single ADC used to digitize a cellular spectrum, b) efficient channelizers utilized for extracting individual signals from the wide-band signal. Authors have also presented a new computationally efficient wide-band channelizer known as opened filter bank (OFB) channelizer, which was closely related to the DFT filter bank which is used in transmultiplexers. OFB channelizerwas less complex than canonical DFT filter. Yoshida, Otaka, Kato and Tsurumi (2000)[12] developed a SDR using direct conversion principle. An analog quadrature demodulator with fixed frequency local oscillator was organized for every band and was used to down convert entire channel bandwidth to baseband. The two characteristics required for analog stage to down convert the entire channel bandwidthto the baseband of different communication systemswith different frequency band, are: a) Multi-band characteristic,b) Broadband characteristic. The developed SDR receiver was realized multiband characteristics at 1.5 GHz and 1.9 GHz band and broadband characteristic up to 10 MHz together with demodulation function of quadrature phase shift keying (QPSK) and gaussian minimum shift keying (GMSK). Improvement in design could be achieved by balancing the quadrature demodulator in order to increase the image cancel ratio. Harrisand Rice (2001)[13]proposed poly phase filter banks for symbol timing synchronization in SDR. The poly phase filter bank have separated interpolation and matched filters. No interpolation filter was required after the matched filter, which provided a usual way to include maximum likelihood timing estimation into the loop. Moreover, the samples produced were aligned by frequency as well as phase with the data clock. Authors have also proved the equivalency of polyphase indexing to the fractional interpolation interval. ADC was not allowed to be put up at intermediate frequency due to high phase noise in this approach. Fung and Chan (2002)[14] presented a channelizer using multistage FB for software radio base stations. It was implemented by efficient sample rate changers and several stages of DFTFBs. The polyphase filter in the channelizer was implemented using SOPOT or CSD technique to represent the filter coefficients. Thus, coefficients multiplications were implemented by minimum number of additions and shifts only. Furthermore, an efficient technique called multiplier-block was used to implement the multiplier less FB with minimum number of adders. The channels had different bandwidths which were isolated from each other using this multistage method repeatedly. The presented method was more flexible to receive different bandwidth channels as needed in a multi-standard base station of mobile communication system and implemented with reduce computational complexity. The complexity of the design is slightly higher than the conventional design because of additional computational load at SRC. Xu, Wu and Bosisio (2003)[15] designed a SDR architecture using Six Port technology or multi-port demodulator to provide multimode and multi-channel wireless receiver. Six-port was consisted by interconnecting combiners and dividers in such a way that the signal which has to be measured along with four different sums of reference signal was produced. The results of the actual integrated SDR and Six-Port technology circuit provided low cost system, large flexibility in system design, and also huge potential for software reuse. Schnepp, Muller, Luyand Russer(2003)[16] implemented channel diversity for mobile SRR. It overcomes the received signal distortion due to multipath fading. The technique was based on Software Radio architecture, so the technique was easily extended to more communication channels. A coherent superposition of multiple information from different transmitters at different frequencies to increase the reception quality was implemented in this technique. Moreover, presented technique was an alternative to antenna diversity and it resulted in reduced number of antennas. However, there was fading effect in the superposed signal due to doppler frequencies from different transmitter. Yeung and Chan (2004)[17]presented multiplier-less realization and design of SRR with reduced system delay. Authors studied two approaches; a) multiplier-less hardware realization, b) realize the SRR using DSP. The SRR's fixed coefficients were implemented efficiently with fewer numbers of additions and shifts using the SOPOT representations. The design was implemented by applying digital all pass filters and low delay FIR filters that significantly decreased the system delay of the multistage decimators in SRRs. In the conventional SRR to avoid the need of costly programmable FIR filter, the Sampling Rate Converter (SRC) was used. This SRC was implemented using a variable digital filter immediately after the integer decimators. Hence, the design has reduced system delay and implementation complexities. Xu, Bosisio and Wu (2005)[18] proposed a SRR platform which is based on Substrate Integrated Waveguide (SIW) six-port structure. The structure was compact and had lower cost. It did not require any external terminal as conventional six port structure. The operating frequency of receiver was from 22GHz to 26GHz for different modulations. The simulation results proved that the platform based on six-port technology was flexible and stable in system configuration, which could be used in software defined radio applications. Kruth, Simon, Dufrene, Weigel, Boos and Heinen (2006)[19]designed a flexible and low power front end for multimode SRR. The major problems of SRR were; a) narrowband LNA with different noise figure specification as well as linearity b) front end filtering for each communication systems. The designed SRR covered entire frequency with gain switches by wideband common gate LNA2, which offered a high linearity downconverter current mode interface between baseband filter and mixer with 32mA at1.5V power supply. The noise due to the basedband section was drastically reduced because the design provided a high voltage conversion gain. Moreover, the receiver also had the broadband frequency characteristics; hence, it was used in various communication standards like Global System for Mobile (GSM), Code Division Multiple Access (CDMA) and Wideband Code Division Multiple Access (WCDMA). Mahesh and Vinod (2006)[20] worked on low complexity reconfigurable FIR filters for SRR based BCSE. Authors discussed two architectures for the implementation of FIR filters: a)

Implementing FIR filters without using programmable shifter, and b) Programmable shifter was employed in the FIR filters. The later architecture offered a significant reduction in power and was designed to work at a high speed for a 12-bit coefficient of FIR filter with 109.7 MHz as clock frequency on Xilinx's Virtex II FPGA. The architecture results in saving ofaddition operations by 23% in comparison with canonical FIR filter design. Authors failed to analyze the power dissipation issues in designed architecture. Vinod and Lai (2006)[21] presented a design of low power FIR filters havinghigh speed for SRR. Digital FIR filters were designed in this work were having less number of adders for SRR. Details of two different techniques used for its designing are: a) PFP technique was used for encoding of filter coefficients, and b) Technique called Span reduction was used to code filter coefficient with fewer bits than canonical fixed point filters. The design provided average saving in the number of adders used i.e. 80% of full adders and 40% of adders required for the coefficient multipliers as compare to canonical FIR filter designs. Hence, there was reduction in computational complexity of the filter. It was observed that the PFP encoded technique was not an optimal representationHueber, Maurer,Strasser, Stuhlberger, Chabrak, and Hagelauer(2006)[22] implemented a SRR with low system delay and multimode capability for applications in mobile terminal. Authors also discussed design considerations and disadvantages of a digital front end used for multi-mode type of mobile communication and divided the functionality of the digital front end into three parts: a) Sample rate was decreased using the decimation stage by an integer factor relating to anti-aliasing filtering, b) Single user channel was extracted using channel filtering, and c) Sample rate decreased using fractional SRC by a non-integer factor. The challenges related with multimode capable terminals were solved by efficient design of digital front end. The design provided a high reconfigurable, an efficient power consumption and reduced IC area. Abidi (2007)[23] redefined the SRR to tune with one channel of any bandwidth, making SRR a universal receiver in multi-standard wireless communication. Further, the cascaded anti alias filters significantly eliminate the unwanted channels as the high decimation factor which was distributed over two or more stages. The power and dynamic range of the ADC was reduced. The design is more flexible than used in conventional receivers as the user selected both decimation factor and number of stages. Author also developed a wideband LNA of 90-nm Complementary Metal Oxide Semiconductor (CMOS) sample tuned to 200 kHz to 20 MHz channels placed anywhere between 800 MHz to 6 GHz,but did not find hardware efficient way of receiving several continuously transmitted channels like CDMA. Araujo and Dinis (2007)[24]presentedan analytical approach to evaluate quantization effects in ADC which is used in SRR design. Authors used multiband/multiuser signal as input of a wideband ADC and took benefit of Gaussian behavior of the signal. Moreover, it was used for performance evaluation and optimizingthe quantization characteristic of ADC in computationally efficient way. An improvement in SIR level of several decibels was achieved by using oversampling factor and reference frequency. Awan, Alam, Koch and Behjou(2007)[25] presented design and implementation of Multi Standard SRR based on FPGA. RF signal after LNA was directly sampled at 840 MHz by bandpass sampling technique. Moreover, the front end processed different signal in the digital domain, which removed the hardware limitations as presented by conventional design. Polyphasechannelizers were used for extracting channels of 12 Universal Mobile Telecommunications System (UMTS) and 3 Wireless Local Area Network (WLAN) with desired rate at the baseband. The design was implemented using different structural techniques. Serial Polyphase filter with parallel Multiplier and Accumulator (MAC) was used for given design. By critically analyzing the design in terms of hardware, it is proved that the Distributed Arithmetic or Xilinx DSP48 blocks were efficient and best for implementing the polyphasechannelizer. However, there was need of various standard polyphase channelizers to extract all the channels. Mahesh and Vinod (2007)[26] worked on implementation of FRM based computational efficient reconfigurable channel filters for SRR. Designhas decreased the complexity of the filter by minimization of precision coefficient without affecting the output of the filter. It offered a 37% reduction in adder over BSE based approach and 57% over CSD based approach. The method was tested on multiple levels of reconfigurability. Moreover, the architecture required large amount of hardware resource which made this infeasible for SRRs. Chan, Tsui, Yeung and Yuk(2007)[27]designed a digital IF architecture for SRR. It includes the digital filters having fixed coefficients and limited multiplier required in SRC. The fixed coefficient filters were implemented using SOPOT coefficients and Multiplier Block (MB) technique to reduce the computational complexity. Two algorithms were presented to optimize the internal wordlengths of Linear Time Invariant (LTI) systems subject to prescribed output accuracy: a) A closed solution was found using the Lagrange multiplier method, and b) The desire wordlengths found in the integer values using Marginal analysis method. It was implemented without any multiplications and there was a trade-off between the hardware complexity & the filter performance. Farhang-Boroujeny (2008)[28] worked on FBs as a means for sensing a spectrum in CR systems. Farhang-Boroujeny suggested different types of FBs and also evaluated their performance through theoretically and numerical examples. The advantages and disadvantages of given spectrum analyzer and Thomson's MT method were also discussed by comparing these two approaches. The stress was given on the FBs whose main task was to make possible communications which had multicarrier. In such cases, the sensing of spectrum came at almost no additional cost, as the FB which was used for demodulation that was also used for analysis of signal. Thomson's MT method has limited application in Cognitive Radios (CRs) because of computational cost. Analysis of spectrum done by designed FB on the other way was more efficient. Mirzaei, Chehrazi, Bagheri and Abidi(2009)[29]synthesized and designed a second order filter for a SRR. The designed filter attenuated aliasing blocker before sampling. Designed filter was superior to first order filter due to its advantages: a) Exclusion of decimation stages, b) Initial rate of sampling was lower, c) Simple clocking scheme. Authors also studied various imperfections like gain mismatch, transconductor output impedance, and residual offsets in the channels by analyzing the noise and linearity performance of the filter. Moreover, it was observed that the filter was robust to clock jitter and suited for flicker noise cancellation. It offered comparable power consumption in spite of six transconductors. Mahesh and Vinod (2011)[30]introduced a computational efficient, flexible and

reconfigurable FBs for both non-uniform and uniform channelization in SRR using coefficient decimation. Their FBs were capable to receive channels of various communication standards at same time, whereas opposite to this DFTFB based receiver required separate FBs for parallel reception of multiple communication standard channels. The proposed method was focused on SRR application and was employed to all scenarios where DFTFB was used. In this paper emphasis should be given on energy consumption by the SRR. Mahesh, Vinod, Lai and Omondi (2011)[31] suggested the use of FB channelizes for multi-standard SRR. These FB architectures best than existing ones in terms of both dynamic re-configurability and low complexity which are key requirements in SRR. FRM based FB gave more précised results and was an efficient replacement for the per-channel method. Coefficient Decimation method based FB had less computational complexity and was a substitute for DFTFBs. FB had complete control over the passband locations and passband width. There was reconfiguration overhead due to the use of masking filter. Cruz, and Carvalho(2011)[32]presented a design in which dynamic range of ADC was increased in SRR without using more number of components and flexibility. The design increased the dynamic range of ADC which was equal to the value of the attenuator used. Moreover, the flexibility property of the design allowed it to use in bandpass sampling and variety of receivers with same complexity of front end. The design was used for wide band receiver in SDR. However, it consumed more DC power and nonlinear distortion because it was based on active devices. Moreover, the design showed improvements in performance, when two different modulated signals were used for simulations. In this design, 10 dB increase in the dynamic range was achieved which was controlled by the attenuator. Complexity of the model could be optimized by the tradeoff between number of devices and outcome. George, Elias(2012)[33] presented a sharp FIR filter which has continuously variable bandwidth with low complexity and low distortion. The two random SRCs were combined to obtain fixed length filter which was having continuously variable bandwidth. The sample rate was varied by the first SRC as per the need of the efficient bandwidth. The output of first SRC was processed in a filter having fixed length and bandwidth. Further, the initial rate of sample was recovered by applying output of the filter to second SRC. This efficiently changed filter's bandwidth which was required in SRR to fine tune at desired channel. FRM technique was used to design fixed length FIR filter with sharpness and low complexity. Hence high performance as well as saving in the computational complexity was achieved in SRR, however hardware complexity of the filter increases. Deng, Huang, Liu, Li, Huang, and Yi (2013)[34] designed and implemented both ADC and Digital down Converter (DDC) in system on chip for IF digital SRR. In this design, IF analog signal transformed into baseband digital signal. Hence,design made the SRR system higher integrated, more flexible and reliable as compared to the combination of DSP and FPGA functions. Further, the data was accepted at 200 MHz sample rate by System on Chip (SoC). Simulation outcomes showed that the design worked well for different types of wireless applications. George, Elias(2014)[35] design a channelizer in which variable bandwidth filter is used to reduce or enhance the bandwidth without any change in the filter coefficient. The designed channelizer can convert wideband channel in to baseband channel without using intermediate stage. The computational complexity of FRM channelizer was reduced by representing filter coefficient in canonic signed digit representation which was optimized by using nature inspired modified harmony search. Hence, the power consumed by the channelizer was reduced. The channelizer also helped to reduce the gap between DSP and antenna of SRR. The designed filter was also known as selectable bandwidth filterAmbede, Shreejith, Vinod, and Fahmy (2015)[36] presented method for designing variable digital filter in SRR channelizer which have less computational complexity. The method named as improved coefficient decimation. Varieties of responses were obtained using same set of filter coefficients. There was limitation to achieve sharp transition bandwidths (BWs) because the filter required high order for this and hence, the computational complexity of filter may increase. Kalathil, Elias(2016)[37]designed near perfect construction (NPR) non-uniform cosine modulated FB using frequency response masking technique. The hardware complexity of filter is decreased by utilizing canonic signed digit representation of filter coefficient and further optimized by using hybrid GSA-HSA algorithm which is the combination of two modified metaheuristic algorithms i.e. Harmony search algorithm (HSA) and Gravitational Search algorithm (GSA). Hybrid algorithms have the properties of both metaheuristic algorithms. The resulting FB has low complexity and sharp transition width. The designed filter bank was used as a channlizer in SDR receiver. It has problem of linear phase. Sakthivel,Elias (2018)[38]presented digital channelizersfor SDR using NPRnon-uniform modified Discrete Fourier transform FB. The designed filter used frequency masking technique along with common subexpression elimination method, multiobjective artificial bee colony optimization algorithm, canonic signed digit representation and modified shift inclusive differential technique to obtain less hardware complexity and narrow transition width. As compare to cosine modulated filter banks the proposed filter have linear phase and less hardware complexity. Authors have implemented the proposed filter on FPGA. Akeela and Dezfouli(2018)[39] have given broad overview of the variety of design methods and hardware platforms implemented for SDR. This paper incorporates FPGAs, GPPs, DSPs, GPUs, and co-design. Authors discussed the basic architectures and investigated their disadvantages and advantages. They have compared design approaches by considering power efficiency and computational power and also discussed different issues related to SDR which is helpful to developed advanced SDRs.

3. Observations based on study of SDR or SRR design techniques

From the survey the following analysis have been drawn:

a) The basic idea of SDR is to provide flexibility to communication system through the property of reconfigurability by substituting the analog signal processing with digital signal processing. So, for implementing SDR architecture, low complexity as well as flexibility are required for filter. The complexity of the filter is reduced by modifying the coefficients.

b) SDR means that different communication standard can communicate with each other using same hardware by reprogramming or reconfiguring using appropriate software. SDR must be design such that it has low power consumption and high speed.

c) SDR can considerably reduce the complexity and cost of base stations for wireless communication system. In SDR wideband ADC and DAC are used as close to antenna as possible. Digital domain is used for all signal processing and functionality.
d) Channelizer is the most computationally concentrated block in SRR which is used in the digital front end. Channelizer is implemented using high speed and low power FIR filters. Delay, multiplier and adder are the key functional units of a digital filter. Multiplier deals with the arithmetic complexity of filter which is important in channelizer. Multiplications in filtering operation are easily replaced with shift and add by different techniques.
e) Direct digitization of FM band can be done immediately after the LNA using channel diversity. Channel diversity is achieved by extracting the different channel from the same source as result of filtering and downsampling the broadband signal.
f) There is a need to design optimal filter for channel separation in SRR. This process removes nearby channels for the wideband signals without affecting band of interest.
g) SRR required variable bandwidth or variable frequency response characteristics. There is change in the bandwidth or frequency response of FIR filter by changing the order of a filter which is a common method. According to this method, there is a reduction in bandwidth or frequency response with increase in filter order or tap and vice versa.

4. CONCLUSION

From the survey it has been concluded that there is a need to develop and implement a FIR filter with optimized symbol detection for SRR to reduce noise and extracting different channels in multi-standard communication system. The emphases are to improve the computational complexity, reconfigurability and power consumption. SRR is becoming superior to other technology due to its ability to extract different narrowband channels form wideband channel with high level of flexibility and reconfigurability at same time. Digital filter is an important part of SRR. Hence, there is a need to investigate DSP wireless communication systems in which digital filter is specifically designed to provide less computational complexity with lower power consumption. FIR filter designed by changing the filter coefficients is widely used and further can be optimized using different types of algorithms.

REFERENCES

[1] Mitola, J. III (1992), “Software Radios - Survey, Critical Evaluation and Future Directions”, IEEE National Telesystems Conference, Washington, DC, pp. 15-23.
[2] Mitola, J. (1995), “The Software Radio Architecture”, IEEE Communications Magazine, 33(5), pp. 26–38.
[3] Mitola, J. III (2000), Software Radio Architecture: Object-Oriented Approaches to Wireless Systems Engineering, New York: John Wiley and Sons.
[4] Mitola, J. III (2000), “Software Radio Architecture Evolution- Foundations, Technology Tradeoffs, and Architecture Implications”, IEICE Transactions on Communication, 6, pp. 1165-1173.
[5] Mitola J. III (2000), “Technical Challenges in the Globalization of Software Radio”, IEEE Communications Magazine, 37(2), pp.84-89.
[6] Reed, J. H. (2002), Software Radio: A modern Approach to Radio Engineering, New Jersey: Prentice Hall PTR.
[7] Poole, Ian, “Software Defined Radio (SDR), Tutorial” from web site http://www.radio-electronics.com/info/rf-technology design/sdr/software-defined-radios-tutorial.php.
[8] Menon, A. and Gopisetty, A. (2011), “Project SDR: Remote Terminal Access Control System”, from the web site http://www.ece.cmu.edu/~ee51/projects/S11/Group7S11.pdf
[9] Zangi, K. C., and Koilpillai, R. D. (1998), “Efficient FilterbankChannelizers for Software Radio Receivers”, IEEE International Conference on Acoustics, Speech and Signal Processing, Seattle, WA, 6, pp. 3497 - 3500.
[10] Seskar, I. P. and Mandayam, N. B. (1999), “A Software Radio Architecture for Linear Multiuser Detection”, Journal on Selected Areas in Communications, 17(5), pp. 814-823.
[11] Zangi, K. C. and Koilpillai, R. D. (1999), “Software Radio Issues in Cellular Base Stations,” IEEE Journal on Selected Areas in Communications, 17(4), pp. 561-573.
[12] Yoshida, H. Otaka, S., Kato, T. and Tsurumi, H. (2000), “A Software Defined Radio Receiver using the Direct Conversion Principle: Implementation and Evaluation”, IEEE International Symposium on Personal, Indoor and Mobile Radio Communications, London, 2, pp.1044-1048.
[13] Harris, F. J. and Rice, M. (2000), “Multirate Digital Filters for Symbol Timing Synchronization in Software Defined Radios”, Journal on Selected Areas in Communications, 19(12), pp.2346-2357.
[14] Fung, C.Y. and Chan, S.C. (2002), “A Multistage Filter Bank based Channelizer and its Multiplier-Less Realization”, IEEE International Symposium on Circuits and Systems, 3, pp. 429-432.
[15] Xu, X., Wu, K. and Bosisio, R. G. (2003), “Software Defined Radio Receiver Based on Six-Port Technology”, IEEE MTT-S International Microwave Symposium Digest, Philadelphia, USA, 2, pp.1059-1062.
[16] Schnepp, H., Muller, T., Luy, J. F.and Russer, P. (2003), “The Implementation of Channel Diversity in Mobile Software Radio Receivers”, IEEE Microwave and Wireless Components Letters, 13(8), pp. 323-325.
[17] Yeung, K. S. and Chan, S. C. (2004), “The Design and Multiplier-less Realization of Software Radio Receivers with Reduced System Delay”, IEEE Transactions on Circuits and Systems-I: Regular Papers, 51(12), pp.2444-2459.
[18] Xu, X. R., Bosisio, G. and Ke, W. (2005), “Analysis and Implementation of Software Defined Radio Receiver Platform”, Asia-Pacific Microwave Conference Proceedings, 5.
[19] Kruth, A., Simon, M., Dufrene, K., Weigel, R., Boos, Z. and Heinen, S. (2006), “A Multimode Receiver Front-end for Software Defined Radio”, Proceedings of European Conference on Wireless Technology, Manchester UK, 5(2), pp.19-22.
[20] Mahesh, R. and Vinod, A. P. (2006), “Reconfigurable Low Complexity FIR Filters for Software Radio Receivers,” IEEE International Symposium on Personal Indoor and Mobile Radio Communications, Helsinki, Finland, pp. 1-5.
[21] Vinod, A. P. and Lai, Edmund M. K. (2006), “Low Power and High-Speed Implementation of Fir Filters for Software Defined Radio Receivers”, IEEE Transactions on Wireless Communications, 5(7), pp.1669-1675.

[22] Hueber G., Maurer, L.,Strasser, G., Stuhlberger, R., Chabrak, K. and Hagelauer, R.(2006), "The Design of a Multi-Mode/Multi-System Capable Software Radio Receiver", IEEE International Symposium on Circuits and Systems, Island of KOS, pp.3958-3961.
[23] Abidi, A. A. (2007), "The Path to the Software-Defined Radio Receiver", IEEE Journal of Solid State Circuits, 42(5), pp.954-966.
[24] Araujo, T. and Dinis, R. (2007) "Analytical Evaluation and Optimization of the Analog-to-Digital Converter in Software Radio Architectures", IEEE Transactions on Vehicular Technology, 56(4), pp.1964-1970.
[25] Awan, M. U. R., Alam, M. M., Koch, P. and Behjou, N. (2007), "Design and Implementation of an FPGA-based Multi-standard Software Radio Receiver", Norchip Conference, Aalborg, pp.1-5.
[26] Mahesh, R. and Vinod, A. P. (2007), "Frequency Response Masking Based Reconfigurable Channel Filters For Software Radio Receivers", IEEE International Symposium on Circuits and Systems, New Orleans, LA, pp.2518-2521.
[27] Chan, S.C., Tsui, K. M., Yeung, K. S. and Yuk, T. I. (2007), "Design and Complexity Optimization of a New Digital IF for Software Radio Receivers with Prescribed Output Accuracy", IEEE Transactions on Circuits And Systems—I: Regular Papers, 54(2), pp 351-366.
[28] Farhang-Boroujeny, B. (2008), "Filter Bank Spectrum Sensing for Cognitive Radios", IEEE Transactions on Signal Processing, 56(5), pp.1801-1811.
[29] Mirzaei, A., Chehrazi, S., Bagheri, R. and Abidi, A. A. (2009), "A Second-Order Antialiasing Prefilter for a Software-Defined Radio Receiver", IEEE Transactions on Circuits and Systems—I: Regular Papers, 56(7), pp.1513-1524.
[30] Mahesh, R. and Vinod A. P. (2011), "Low Complexity Flexible Filter Banks for Uniform and Non-Uniform Channelization in Software Radios Using Coefficient Decimation", IET on Circuits, Devices and Systems, 5(3), pp. 232-242.
[31] Mahesh, R., Vinod, A. P. Lai, E., M. K. andOmondi, A. (2011), "Filter Bank Channelizers for Multi-Standard Software Defined Radio Receivers," Journal of Signal Processing Systems, 62(2), pp.157-171.
[32] Cruz, P. M. and Carvalho, N. B. (2011), "Enhanced Architecture to increase the Dynamic range of SDR Receivers", IEEE Radio and Wireless Symposium, Phoenix, AZ, pp.331-334.
[33] George, J. T. and Elias E. (2012), "Continuously Variable Bandwidth Sharp FIR Filters with Low Complexity", Journal of Signal and Information Processing, 3(3), pp. 308-315.
[34] Deng, J., Huang, X., Liu, L., Li, Y., Huang, X., and Tao, Y. (2013),"Design and Implementation of a Mixed SoC for IF Digital Software Radio Receiver", Sixth International Conference on Advanced Computational Intelligence, Hangzhou, China, pp. 262-265.
[35] George, J. T., Elias, Elizabeth (2014), "Reconfigurable channel filtering and digital down conversion in optimal CSD space for software defined radio", International Journal of Electronics and Communications, 68, pp.312-321.
[36] Ambede, A.,Shreejith, S., Vinod, A. P. and Fahmy, S. A. (2015), "Design and Realization of Variable Digital Filters for Software Defined Radio Channelizers using Improved Coefficient Decimation Method", IEEE Transaction Circuits System II, 63(1), pp. 59-63.
[37] Kalathil S. Elias, E.(2016), "Design of multiplier-less sharp non-uniform cosine modulated filter banks for efficient channelizers in software defined radio", Journal of Engineering Science and Technology,19, pp.147-160.
[38] Sakthivel, V., Elizabeth, E.(2018), "Low complexity reconfigurable channelizers using non-uniform filter banks", Journal of Computer and Electrical Engineering,68, pp.389-403.
[39] Akeela, R., Dezfouli, B.(2018), "Software-defined Radios: Architecture, state-of-the-art, and challenges" Journal of Computer Communications,128,pp.106-125.