MODELING OF ACTIVE SHIELDING ON-CHIP INTERCONNECTS FOR REDUCED CROSSTALK EFFECTS

R.Sridevi, Dr. P.Chandrasekhar

Abstract: An Efficient geometry with active shielding for Coupled RLC interconnects driven by a CMOS gate for crosstalk reduction has been presented in this paper. Two RLC interconnects have been used as shields on both sides of the victim line while maintaining minimum area and power requirements. Shielded interconnect lines are modeled using FDTD technique and the model proposed is validated using HSPICE simulations for 32nm technology. From the transient responses for different switching cases on the proposed geometry, it can be observed that the outcomes using HSPICE and FDTD modeling differ by very small value of less than 5%. The results indicate that crosstalk effects like crosstalk noise, noise peak and power dissipation are reduced considerably using shields between interconnects by 66.6%, 20%, 32%, 40% when compared with unshielded interconnect lines.

Index Terms: Active shield, Crosstalk noise, CMOS driver, Delay, HSPICE, FDTD, RLC interconnects

1 INTRODUCTION

Advancements of technology have led to high speed, high density complex VLSI circuits. Complex VLSI chips designing need integration of millions of components and closely spaced interconnects on a single chip. To achieve higher packaging density and smaller chip area with shorter transmission times multilayer interconnects are desirable. Denser and miniaturized chips require interconnects with reduced lengths in local levels and longer distance interconnects in global level to deal with growth in chip sizes and functional density. Thus interconnects play a vital role in the chip performance in terms of delay, power dissipation, signal integrity and noise. According to ITRS (International Technology Roadmap for Semiconductors) [1] RLC interconnect delays dominate gate delays in advanced technology nodes. Increase in chip density has led to much tightly coupled interconnects with reduced cross sections, resulting in unwanted crosstalk interference between adjacent lines [2].

Crosstalk can be defined as the electromagnetic coupling of signal from one conductor to another. Crosstalk can be classified into two types i) mutual inductance ii) mutual capacitance. Interconnects adjacent to each other are said to be magnetically or inductively coupled, when the change in current in one interconnect induces voltage on other adjacent lines. With increase in chip speeds, inductive coupling has increased. Electrostatic coupling between two interconnects due the electric voltages on the lines led to capacitive coupling. These inductive and capacitive couplings become significant with shrinkage of geometries. Logic failures due induced voltage spikes, increase in delay and distorted signals are the side effects of coupling.

Performance of on chip interconnects is analyzed considering them as distributed RLC interconnects. Effects on coupled transmission lines driven by linear resistor was proposed by Agarwal [3] and Kaushik [4] has extended this model with a non-linear CMOS driver using alpha power law for analyzing functional and dynamic crosstalk effects[5]. In [3-5] models were proposed for transient analysis of lossless coupled interconnect lines which is impractical. Earlier interconnects were modeled representing CMOS gate by a simple resistor as a driver [3]. But accurate estimation of crosstalk noise with linear resistor is not possible because MOSFET operates in both linear and saturation region and in saturation region transistor can be modeled as a current source with high resistance when compared to resistance in linear region, thus leads to errors in performance estimation of driver interconnect load system. Traditionally transmission lines are solved in frequency domain using partial differential equations whereas non-linear elements are described in time domain [6] resulting in frequency to time conversion problem which can be addressed using FDTD technique.

In this paper, focus is on reducing the undesirable effects due to crosstalk in coupled RLC interconnects driven by CMOS gate by providing active shielding [7] between adjacent lines. The major limitation using this technique is increase in area usage for interconnects. FDTD approach is used for modeling coupled lines taking into considering undesirable outcomes due to mutual capacitance and inductance in interconnects. HSPICE simulations are used for validating the proposed approach and the results shown prove that the difference in transient responses using HSPICE an FDTD for 32nm technology is very less about 5%.

The rest of the report is organized as follows: section II describes proposed scheme with active shielding for interconnects. FDTD model is described in section III. The proposed model is validated in section IV using HSPICE and the model is concluded in section V.

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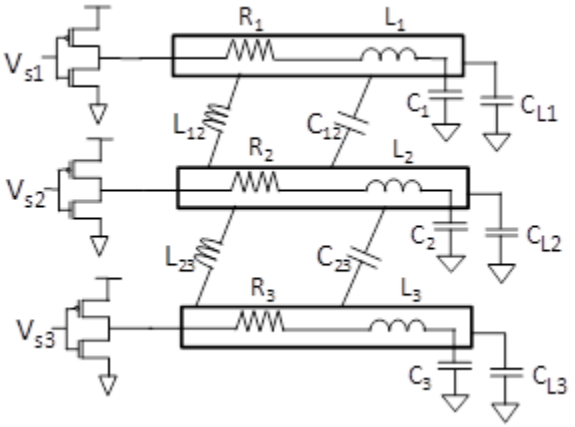

Fig.1 *Coupled RLC interconnects with CMOS driver*

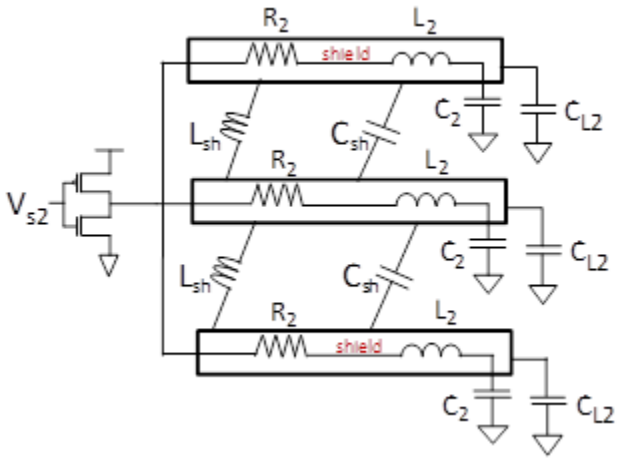

Fig 2 Victim *line with active shielding*

2 ACTIVE SHIELDED MODEL FOR CMOS DRIVEN COUPLED INTERCONNECT LINES

Active shielding is an effective technique for reducing crosstalk noise and delay in interconnects by reducing the capacitive and inductive effects on adjacent lines following Miller effect which states that simultaneous and in phase transitions on adjacent lines result in zero coupling capacitance. Shielding significantly decreases capacitive coupling but moderately decreases inductive coupling because of complexity in forcing the current return path. Active shielding uses dedicated logic circuitry for switching the shield line as per adjacent interconnect line [8] naturally increasing area and power requirements. Shielded lines are driven by the same buffers as that of the desired line for proper synchronization [8]. A CMOS driven interconnect model without and with a shield line inserted between the aggressor and victim lines is shown in Fig. 1 & Fig. 2. In these figures R, L, C, C_L are per unit length resistance, capacitance, inductance and load capacitance of the interconnect lines and C_{12}, C_{23}, L_{12}, L_{23} are mutual capacitance and inductance between the lines. Lines 1 & 3 are the aggressor lines and line 2 is the victim line for which shielding has been provided for crosstalk reduction.

3 PROPOSED FDTD MODEL

Active shielded interconnect lines driven by CMOS inverter and terminated by capacitive load are modeled by FDTD technique [9],[10],[11],[12],13]. CMOS drivers are represented by nth power law model. FDTD technique is used for solving Maxwell's equation where the time dependent partial differentials are discretized using central difference approximations in space and time domains [11].

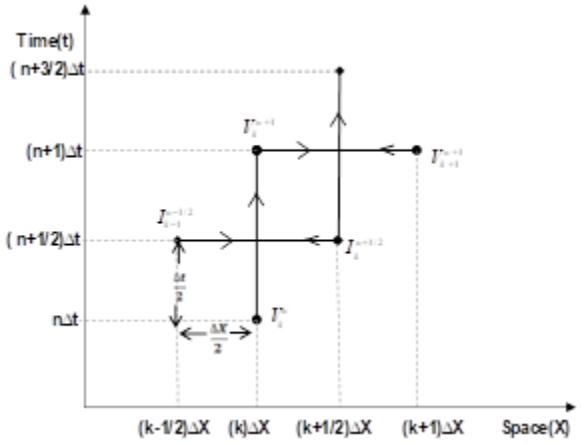

Fig.3 *Discritized voltage and current nodes with respect to space and time*

Fig. 3 shows the relation between voltage and current in time and space domains. As shown in Fig. 3 at any instance of time current in the time domain is dependent on stored value of current in a time domain and on voltage in space and vice-versa.

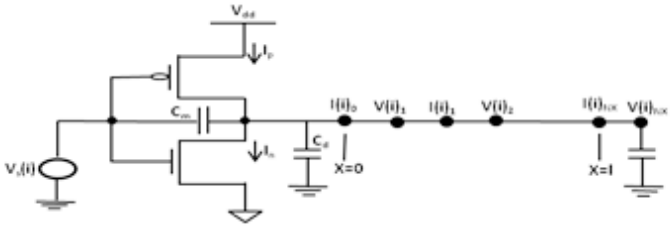

Fig. 4 *Discretized line in space for FDTD analysis*

A interconnect of length L with CMOS driver at X=0 and with a capacitive load at X=L shown in Fig. 4 is

$$\frac{d}{dx}V(x,t) + RI(x,t) + L\frac{d}{t}I(x,t) = 0 \qquad (1)$$

$$\frac{d}{dx}I(x,t) + \frac{d}{dt}CV(x,t) + GV(x,t) = 0 \qquad (2)$$

Where V, I are the line voltages and currents in 3×1 column vectors and the parasitic elements are also represented in 3×3 matrix for p.u.l as

$$V = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}, \quad I = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix}, R = \begin{bmatrix} R_1 & 0 & 0 \\ 0 & R_2 & 0 \\ 0 & 0 & R_3 \end{bmatrix}$$

$$L = \begin{bmatrix} L_{11} & L_{12} & L_{13} \\ L_{21} & L_{22} & L_{23} \\ L_{31} & L_{32} & L_{33} \end{bmatrix} \quad \text{and}$$

$$C=\begin{bmatrix} C_{11}+C_{12} & -C_{12} & C_{13} \\ -C_{21} & C_{22+}C_{12}+C_{23} & -C_{23} \\ C_{31} & -C_{32} & C_{33} \end{bmatrix}$$

On applying central differential approximation on equations (1) & (2) we get

$$\frac{V_{k+1}^{n+1}-V_k^{n+1}}{\Delta X}+L\frac{I_k^{n+3/2}-I_k^{n+1/2}}{\Delta t}+R\frac{I_k^{n+3/2}+I_k^{n+3/2}}{2}=0 \quad (3)$$

for K =1, 2, 3, ……., NI

$$I_k^{n+3/2}=BDI_k^{n+1/2}+A(V_k^{n+1}-V_{k+1}^{n+1}) \quad (4)$$

for k=1,2,3,….NX and

where $B=inv\left(\frac{\Delta X}{\Delta t}L+\frac{\Delta X}{2}R\right),\ D=\left(\frac{\Delta X}{\Delta t}L-\frac{\Delta X}{2}R\right)$

$$\frac{I_k^{n+1/2}-I_{k-1}^{n+1/2}}{\Delta X}+C\frac{V_k^{n+1}-V_k^n}{\Delta t}=0 \quad (5)$$

$$V_k^{n+1}=V_k^n+A\left[I_{k-1}^{n+1/2}-I_k^{n+1/2}\right] \quad (6)$$

where $A=inv\left(\frac{\Delta X}{\Delta t}\right)C$

for K= 2, 3, 4, ……., NX

Voltage and current for integer values of i, j are represented as

$$V_i^j=V[(i-1)\Delta x, j\Delta t],\quad I_i^j=I[\left(i-\frac{1}{2}\right)\Delta x, j\Delta t]$$

The above expressions represent discretized forms of voltages and currents interleaved in time and space domains. For example, when we consider (6), the present value of V is dependent on the previous value of V and the most recent value of current. At the source end, FDTD analysis is done on a lossy transmission line in the presence of nonlinear CMOS gate as the driver. This nonlinear behavior of CMOS gate is represented using by nth power law model [14] and drain current is defined as a linear function of drain voltage, discretized in the time domain for implementing FDTD analysis. PMOS and NMOS currents In , Ip using nth power law model and discretized in the time domain can be given as

$$I_p=\begin{cases} 0, & (off) \\ I_{dsatp}\left(1+\lambda_p(V_{dd}-V_1)\left(2-\frac{V_{dd}-V_1}{V_{dd}-V_{dsatp}}\right)\frac{V_{dd}-V_1}{V_{dd}-V_{dsatp}}\right), & (\text{lin}) \\ I_{dsatp\left(1+\lambda_p(V_{dd}-V_1)\right)}, & (sat) \end{cases} \quad (8)$$

$$I_n=\begin{cases} 0\ , & (off) \\ I_{dsatn}(1+\lambda_nV_1)\left(2-\frac{V_1}{V_{dsatn}}\right)\frac{V_1}{V_{dsatn}}\ , & (lin) \\ I_{dsatn}(1+\lambda_nV_1), & (sat) \end{cases} \quad (9)$$

V_{tp}, V_{tn} are threshold voltages and λ_p, λ_n are finite drain conductance parameters of NMOS and PMOS transistors

PMOS and NMOS drain saturation voltages and currents are given as

$$V_{dsatp}=k_p(V_{dd}-V_s-V_{tp})^{m_p} \quad (10)$$

$$V_{dsatn}=k_n(V_s-V_{tn})^{m_n} \quad (11)$$

$$I_{dsatp}=\frac{W_p}{L_{eff}}B_p(V_{dd}-V_s-V_{tp})^{n_p} \quad (12)$$

$$I_{dsatn}=\frac{W_n}{L_{eff}}B_n(V_s-V_{tn})^{n_n} \quad (13)$$

B_p, n_p, B_n, n_n are the parameters to control saturation region and the parameters k_p, m_p, k_n, m_n are the parameters that control linear region characteristics, W_p, W_n are the widths and L_{eff} is the effective length of PMOS and NMOS transistors.These model parameters are calculated from the method proposed in [14].

TABLE I

MODEL PARAMETERS FOR 32NM

Parameters	PMOS	NMOS
M	0.0569	0.2111
N	1.0048	0.9150
B	0.00086	0.00194
K	0.3033	0.3693
λ	2.78	0.867
V_t	0.36	0.36

Voltage and current at the source end are given V_1, I_0 .By replacing ΔX by ΔX/2 and k=1 in equation (6) we can get the values of V_1 as

$$V_1^{n+1}=V_1^n+2A\left(I_0^{n+1/2}-I_1^{n+1/2}\right) \quad (14)$$

where $I_0^{n+1/2}=\frac{I_0^{n+1}+I_0^n}{2}$

CMOS driver current I0 at source end can be obtained by applying KCL as

$$I_0=C_m\left(\frac{d(V_s-V_1)}{dt}\right)+I_p+I_n-C_d\frac{dV_1}{dt} \quad (15)$$

Discretizing equation (15) we get

$$I_0^{n+1}=C_m\frac{V_s^{n+1}-V_s^n}{\Delta t}+I_p^{n+1}-I_n^{n+1}-(C_m+C_d)\frac{V_1^{n+1}-V_1^n}{\Delta t} \quad (16)$$

where C_m, C_d are drain to gate coupling capacitance and drain diffusion capacitances

On substituting (16) in (14) we get the value of voltage in discretized form at source end as

$$V_1^{n+1}=V_1^n+HA\left(\frac{C_m}{\Delta t}[V_s^{n+1}-V_s^n]+I_0^n\right)-2HAI_1^{n+1/2}+HA\left(I_p^{n+1}-I_n^{n+1}\right) \quad (17)$$

where $H=\text{inv}(U+\frac{A}{\Delta t}(C_m+C_d))$, U is a 5X5 identity matrix

The voltage at load end terminated by capacitive load is given as

$$V_{NX+1}^{n+1}=V_{NX+1}^n+2A\left(I_{NX+1}^{n+1}-\frac{I_{NX+1}^{n+1}+I_{NX+1}^n}{2}\right) \quad (18)$$

The relation between voltage and current at load end terminated by capacitive load Cl is

$$I_l=C_l\frac{dV_{NX+1}}{dt} \quad (19)$$

Load current in discretized form is given as

$$I_{NX+1}^{n+1}=C_l\frac{(V_{NX+1}^{n+1}-V_{NX+1}^n)}{\Delta t} \quad (20)$$

Substituting (20) in (18) voltages at load in discretized form can be obtained as

$$V_{NX+1}^{n+1}=V_{NX+1}^n+2JA\left(I_{NX+1}^{n+1/2}-\frac{I_{NX+1}^n}{2}\right) \quad (21)$$

Where $j=\left(U+\frac{AC_l}{\Delta t}\right)^{-1}$

Voltages and currents at load and source are evaluated for a specific time using equations (20), (21), (17) and (16). Accurate solutions using FDTD will be obtained if the following two conditions are satisfied (i) spatial increment step ΔX must be small enough to obtain proper resolution (ii) ti

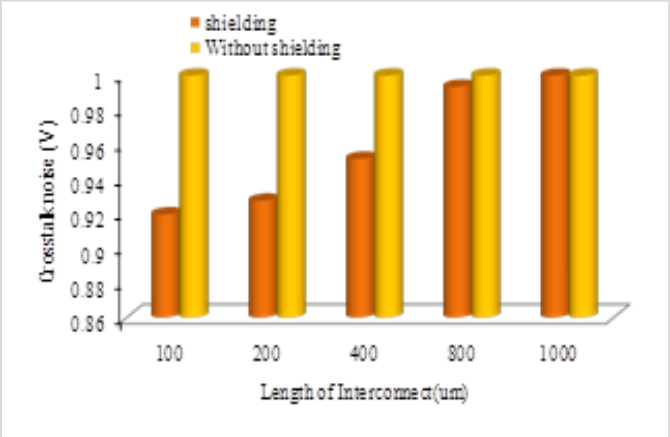

Fig.5 *Functional Crosstalk noise on interconnects*

me and space discretization should follow Courant stability condition [9] given as $\Delta t \leq \Delta X/V$,where V is the velocity of signal on line. According to courant condition the time step should be smaller than the propagation time over each segment. The system has no stability issues as the expressions (17) and (21) are derived following courant condition.

4 PROPOSED MODEL VALIDATION

HSPICE W-element simulations are carried out and compared with the proposed model for validating the model. Parasitic values on interconnects are maintained the same for HSPICE and FDTD implementation for proper synchronization. HSPICE simulations are carried out in 32nm technology with interconnect parasitic chosen as L=2mm, V_{DD}=0.9v, C_L=0.001uF and the ratio of PMOS to NMOS width in CMOS inverter used as driver is chosen as 2. Here coupled three line system is considered where line 1 and 3 are aggressors and line 2 is the victim line. Crosstalk effects on victim line like functional crosstalk effects where victim line is quite and aggressor lines are switching and dynamic crosstalk effects where both aggressor and victim lines are switched simultaneously either in-phase or out of phase manner [15-16] are analyzed and the transient responses are compared with the proposed model at the far end of victim line.

5 RESULTS AND DISCUSSIONS

From the transient response, it's evident that the reduction in crosstalk noise with the proposed model is about 66.6% and the delay has come down by 60% contrast to unshielded interconnect lines. The improvement in performance of interconnects using shielding is substantially good in terms of power consumption, crosstalk noise area, noise peaks, and peak timings when compared with other reduction methods like widening and increasing the lengths of interconnects which lead to increase in resistance, delay and area occupied by interconnects.

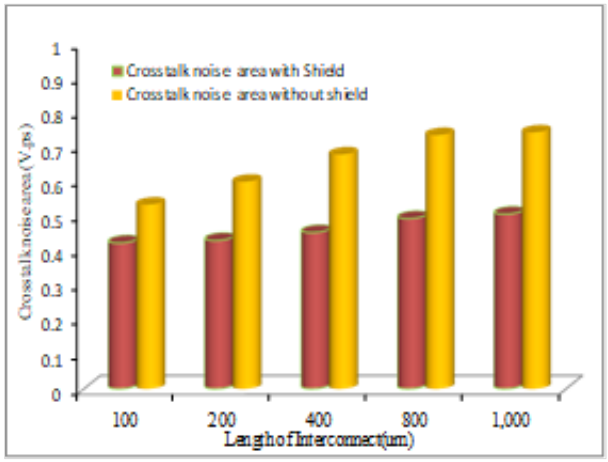

Fig 6 *Crosstalk noise with varying global interconnects length*

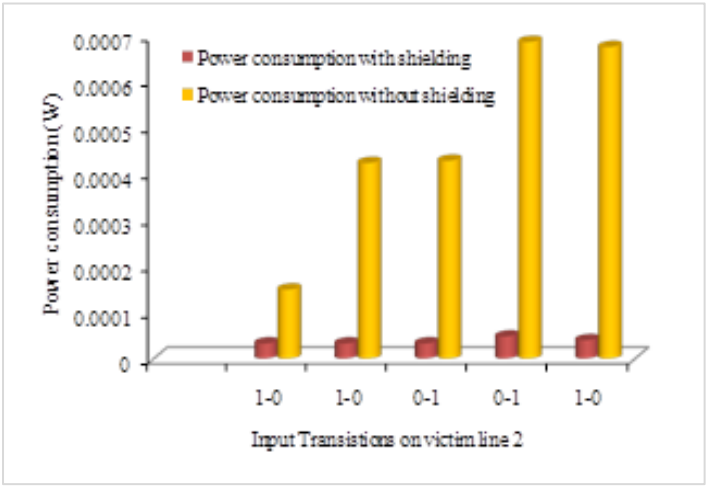

Fig 7 *Crosstalk noise area for global interconnects*

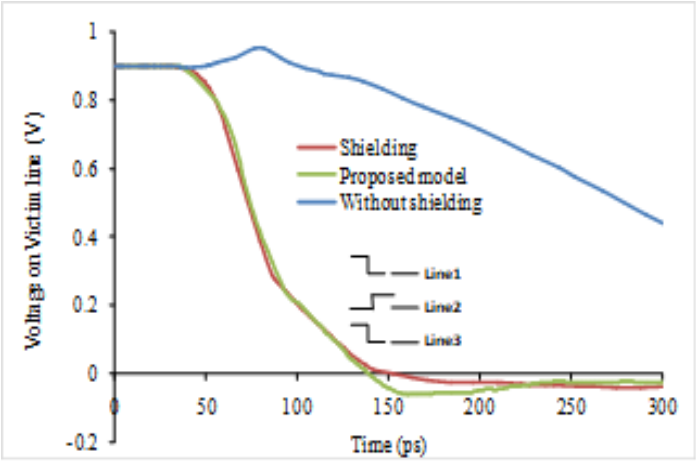

Fig 8 *Power consumption due to transitions on victim line*

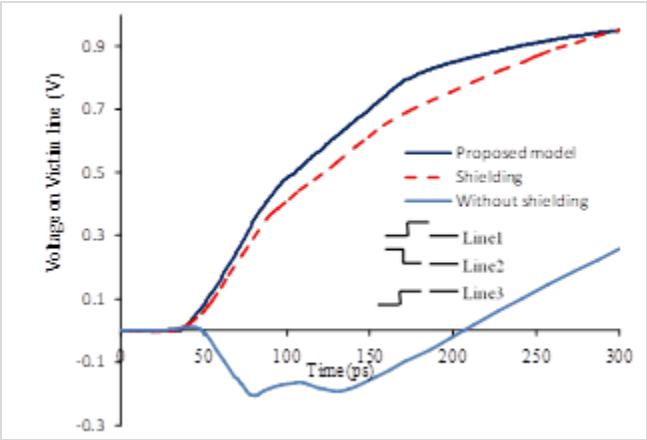

Fig 9(a)

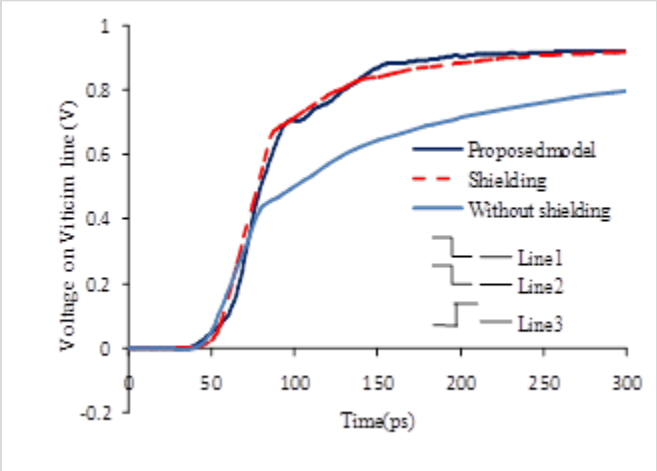

Fig 9(b)

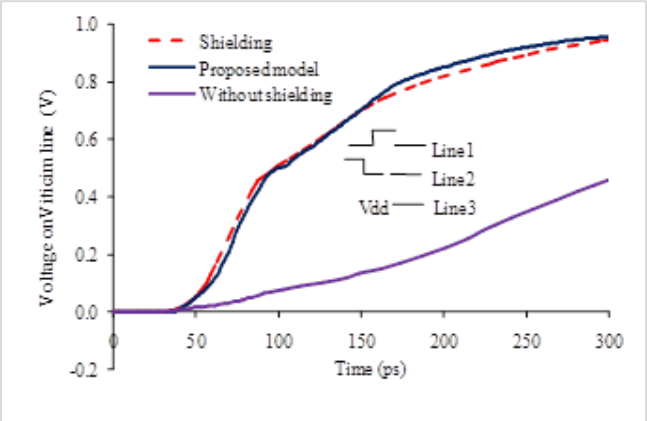

Fig 9(c)

Fig 9 Transient analysis for various input switching conditions on victim line

TABLE II
DYNAMIC CROSSTALK DELAY ON LINE 2

Delay on line 2 (ps)	With Shielding	Without Shielding
In-phase Delay	4.22	4.21
Out-phase delay	5.74	35.5

As shown in Fig. 5, the functional crosstalk noise due to active shielding is less by 66.6% when compared to that of unshielded lines. The primary cause for crosstalk noise is the coupling capacitance that exists between interconnects and it occurs when a victim line is stable at a particular potential and aggressors are switching. This type of crosstalk is known as functional crosstalk and its value is less in shielded lines because the effect of coupling capacitances will be first on shielded lines and later on victim line. Another source of crosstalk noise between interconnects is dynamic crosstalk which occurs due to simultaneous switching between aggressor and victim lines either in-phase or out of phase to each other. Table II gives the values of in phase and out of phase delays for shielded and unshielded lines. As can be observed from table out of phase delay has been reduced by 83%.According to Fig. 6 & Fig. 7, increasing the length of interconnects crosstalk noise peak and crosstalk noise area is reduced and the improvement in noise peak and noise area due to shielding is about 20% and 32% when compared to unshielded lines. As shown in Fig.8 the power consumption on victim line due to switching transitions is reduced by 41% with shielding. Fig. 9 analyzes transient responses on victim line due to shielding and without shielding for different switching cases and can be observed from Fig. 9 that responses due to the proposed model match accurately with that of HSPICE simulations.

5 CONCLUSION

In this paper, we have proposed an effective geometry for coupled interconnect lines with active shielding. The efficiency of the proposed geometry has been verified by comparing crosstalk effects like crosstalk noise, noise area, power consumption, noise peak voltages with unshielded lines. Dynamic crosstalk noise has been reduced considerably using shielding technique as shown in table II. FDTD technique has been used for modeling the CMOS driven active shielded interconnect lines. The proposed model has been validated using HSPICE simulations and the results obtained differ from the proposed model by less than 5%.

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