Comparison Of Parasitic Performance Of Shorted Gate And Independent Gate Finfets

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Abstract: For the RF analog applications, the two variants of FinFETs i.e., Independent gate (IG) and Short-circuited gate (SG) must be analyzed to understand the effect of different biases at the two gates. The variability of the device due to process variations fluctuates in accordance to the FinFET bias, at least for DC output. This paper provides a novel and systematic study of variability focusing on AC parameters in both SG and IG conditions for a 2-dimensional FinFET. Green's Function technique which uses the linearization of the non-linear responses is used to conduct the research utilizing a quasilinear state for the study of nonlinear variability [1], [2]. Study of FinFET's AC variability involves physical and geometric parameters which are most relevant for our analysis, as the parasitics of the FinFET are significantly affected by these parameters. The parasitics also varied with the two variants of the FinFET device.

Index Terms: FinFET, Numerical Simulations, Semiconductor devices, Nanotechnology, Device parasitics

1 Introduction

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) do not comply with Moore's Law any long [2]. In today's world, FinFET innovation is entrenched for computerized applications, and likewise the significance for developing analog RF applications. Within the domain of Independent (IG) Gates or Short-circuited Gates (SG), FinFET operations with fluctuating bias are prone to performance discrepancies in RF analog application investigations and digital applications [3]. The IG variants generally investigated for development of sophisticated circuit topologies exploiting the multi-gate structures [4], [5] whereas the later are explored due to threshold voltage's back-gating effects[6]. The attributes of FinFET AC performance i.e., modeling and simulations are getting popular [3], [5] with the advancement in RF circuits using the peculiar characteristics of multi-gate FinFET. Regardless of optimization and advancement of technology, FinFETs similarly to other nanometer devices get influenced by a great variability resulting from technical or physical parameter variations i.e., doping level, gate work-function and geometrical dimensions. In order to accomplish the FinFETs digital or analog design successfully, modeling of discussed variations is compulsory.

The function of gate bias was only meagerly examined with regard to variability, mostly in direct current conditions. Independent biasing of the FinFET in digital logic circuits have been argued to affect the sensitivity and flexibility of circuits [6].Having said that, AC variability is quite often ignored due to simulation complexity, particularly when it comes to independent gate bias [7]. The unavailability of commercially accessible simulation tools, particularly ones focused on precise physics-based investigation: actually one route to execute RF variability analysis utilizing commercialized TCAD tools such as Synopsys Sentaurus [8], is through repeated system model solutions with varying physical structure via so-called incremental analysis, The model must first be solved for each chosen parameter at the applied DC operating point and then the linearization is performed around the working point, thereby increasing the simulation time significantly. For the numerically effective physics-based simulation of microwave device's AC variability [1], [2], a general structure was recently suggested. This approach is grounded on the Green Function (GF) methodology and provides a substantial time saving in simulations. The new GF method was utilized in analysis of the single and multi-fin FinFET's AC variability, restricted to the state of SG bias[6][7].A detailed study of FinFET AC variability is presented in this report, covering both bias conditions i.e., SG and IG. We demonstrate that as a function of physical parameters with voltage variations at the gate, the sensitivity of Y-matrix components shows inconsistent characteristics. In specific, the variability of the parasitic-dominated AC parameters is less influenced by the bias at the gate, on the other hand the variability in the capacitances of the gate, and in particular of the mutual capacitances of the two gates, is more affected by the disparity in the bias of the gate. This finding is particularly significant while exploiting FinFETs with unbalanced gates for the analog as well as digital applications.

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2 Analysis Of AC Variability – Approach De Green

This work was started with physics-based Large-Signal (LS) mode[9], which allows multi-tone system simulation based on the harmonic balance, including capability of competent GF analysis. To achieve the target of performing AC analysis, we used our simulator is quasi-linear state. On the DC bias of system terminal j: slight AC voltage V_j at the fundamental frequency: as the amplitude of this voltage is minute, the investigation could be restricted to harmonic order n = 0, 1 and only marginally longer than the DC analysis is the simulation time. The AC current of the FinFET device can be calculated at any given terminal, which will affect the AC admittance matrix and we can avoid the need of complex non-linear computation for device analysis. The effect on the device admittance can be shown with the help of following expression.

$$Y(i,j) = Ii / Vj \qquad 1$$

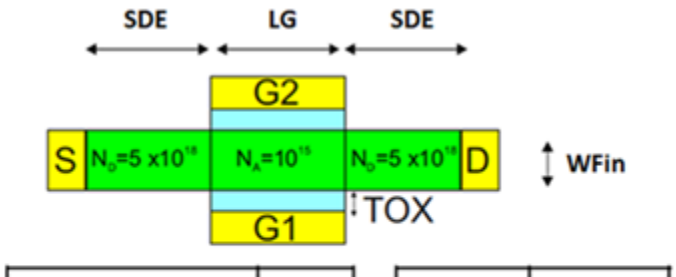
On the basis of this concept, we can evaluate the slight variation in the admittance matrix in response to the variations in the geometry of the device. Let S be the variation parameter representing the minute variations in the geometry and at the constant voltage, the short-circuited current variation is accounted with the help of GF approach. Hence the variation in admittance matrix can be evaluated by:

$$\Delta Y(i,j) = \Delta Ii / Vj \qquad 2$$

Please note that current and voltage are in AC.

3 Variability Analysis For SG And IG FINFET

Fig (1) depicts a single fin Double Gate (DG) composition when applied to the above technique reflecting a FinFET's 2D cross section. The source or drain expansion, source or drain doping, and fin's width are the relevant parameters to be varied. To observe the response of the device, the geometrical as well as doping of the device are varied, since these parameters directly affect the parasitic resistance, thus shaping the performance of the RF system. For the potential applications in the wireless telecommunication networks and advance electronic devices, the considered operating frequency is fixed at 60GHz. Working conditions will be considered with respect to the gate bias: equipotential and independently biased 1gates, these will be referred as SG and IG respectively. With the drain voltage at 1V, we have considered the gate voltage VGS at 0.6 V for the SG case, which results in the drain current of approximately 0.4mA/mm. While for the IG case, the two gates are biased separately. For the comparison of the two cases i.e., the shorted and independently gated devices, we estimated the two biases for the independently biased device as 0.65 V and 0.55 V, hereafter referred as higher gate voltage (GHV) and lower gate voltage (GLV) respectively which provided approximately similar amount of drain current for the two cases.



equivalent SiO_2 TOX	1 nm	LG	54 nm
DE	54 nm	WFin	10 nm

Fig. 1 Structure of DG MOSFET (FinFET)
Metal Gates Si regions SiO2

Listed findings on the AC parameter's sensitivity are shown below for both types of devices. Lines are used for the Green's function approach and Monte Carlo approach (used as a validation) is shown with the symbols. In the IG case, diamonds and triangles are used while SG bias is represented by the circles. For various parameter differences, different colors are used.

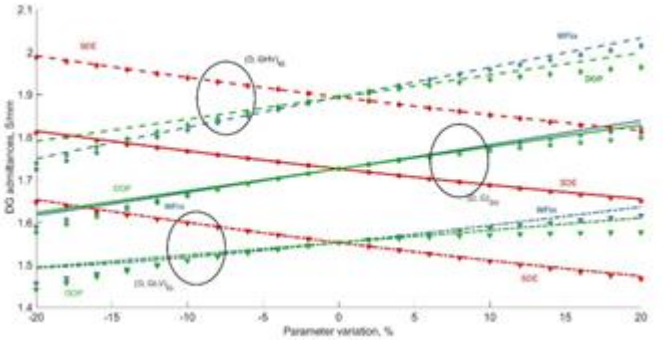


Fig. 2 *Drain-Gate Admittance's real part.*

In Fig (2) against the relative parameter variation, the trans-conductance is shown by the help of plotting the a_{11} element of theY-matrix. As predicted, for both DOP and WFin, a nearly accurate trace of the variations is examined, whereas an opposite pattern is found for SDE [9]. Note that in the case of IG, it is evident that the admittance is different for the drain-gate elements as the applied potential is not similar: lower the voltage at the gate terminal, lower is the trans-conductance. Variations are not sturdily influenced by bias, although the absolute values are different but the curve slope is basically the same: in particular, the readings corresponding to each variance of the parameter are varying with the similar proportionality in the case of both independently driven gate voltage or short-circuited gate voltage; decline in sensitivity can be seen only as a function of DOP and WFin in the (D, GLV) element. Note that, even with parameter fluctuations up to 20 percent with respect to nominal, the precision of the GF method is still excellent.

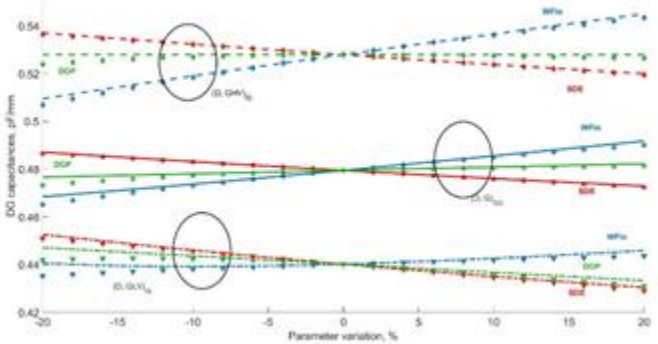


Fig. 3 *Drain Gate Admittance's imaginary part*

Fig (3) illustrates the difference in the admittance matrix of the imaginary constituent of the Drain- Gate (D,G) components. It must be noted that all the imaginary components are normalized by 2πf.Again, in the IG case, the (D,GHV) and (D,GLV) components fluctuate. However, compared to the previous example, the element (D,GHV) shows a greater sensitivity to parameter variations with respect to the (D,GLV)component and is comparable to the SG case. Therefore, this capacitance sensitivity relies on conditions of bias.

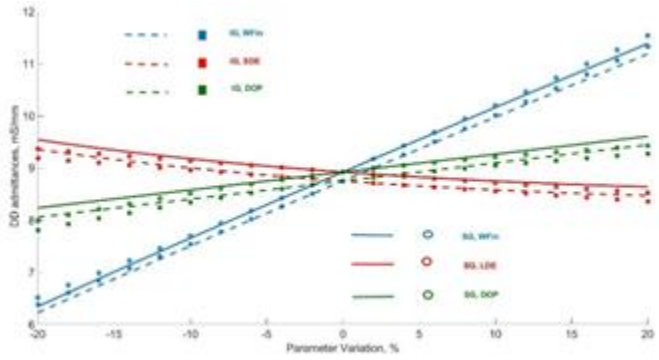


Fig. 4 *Drain- Drain Admittance's real part*

Fig (4) displays the actual part of the admittance matrix components of the Drain-Drain (D,D). Surprisingly, parameter's absolute value is not influenced by the bias of the gate and in all cases the sensitivity also remains unchanged. This can be explained by the fact that these elements are resistive, hence are independent of the bias. Lastly, we examine the behavior of gate capacitances. Fig (5) examines the effect of inter-gate capacitances as they also have adverse effect on the device performance (Note that these capacitances are for single devices and the parasitic capacitances are largely affected by the inter-device capacitances while fabricating the large number of devices on the die).

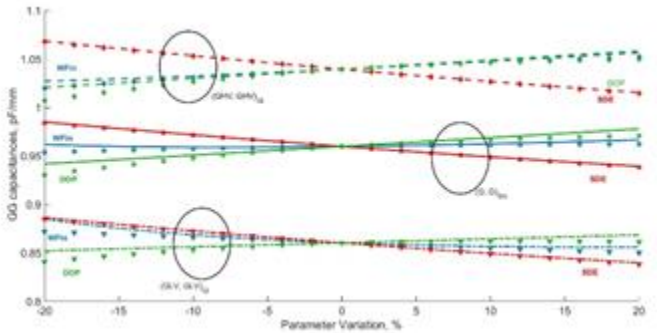


Fig. 5 *Diagonal Gate-Gate Admittance's imaginary part*

The inter-gate capacitances trend is quite complicated. Fig. 5 depicts that the same sensitivity w.r.t., SDE variations. The WFin shows different behavior for the (GHV,GHV) and (GLV,GLV). The sensitivities to DOP variations are identical, whereas the (GLV,GLV) varies. For clarification, in terms of relative variations, the same findings are stated in Fig (6).

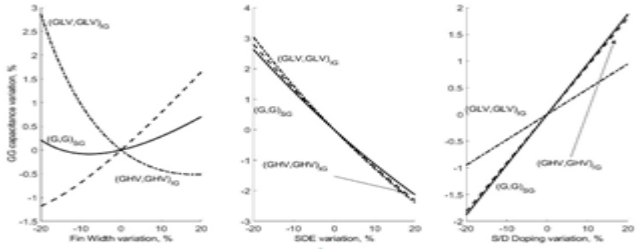


Fig. 6 *Diagonal GG elements of admittance matrix – Percentage variations: Note- Green Function's results are reported only*

Mutual gate capacitance are represented by these components

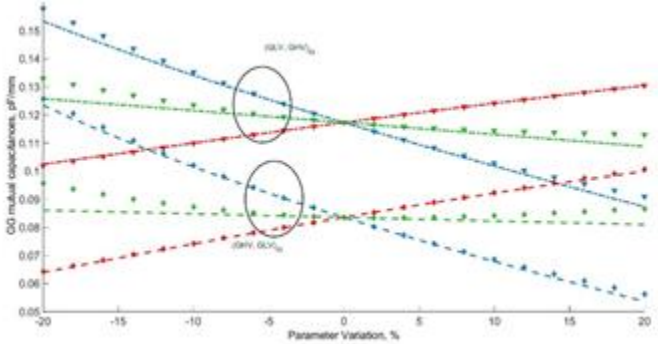


Fig. 7 *Off-diagonal GG components of admittance matrix – Imaginary part (normalized by 2πf)*

Note that their susceptibility to differences is incredibly large; from 20 to 50%, higher than the diagonal components, regardless of their value being smaller than the diagonal components (see Fig. 6). Therefore, it is important to cautiously note the mutual capacitance's variability in RF analog design stages with unbalanced gates. Between the GLV and GHV, the mutual gate capacitances contacts may also play an important role in the case of IG, influencing the RF stage feedback capacitances. Fig (7) demonstrates the sensitivity of parameters of this nature.

4 Conclusions

We have demonstrated the effect of parasitic capacitances and resistances on the both SG and IG variants of FinFET and can conclude that the parasitic capacitances are drastically increased in the case of IG FinFET. Furthermore, the higher computational efficiency is achieved with the help of Greens Function approach. It is recommended that before exploiting IG FinFET for different applications e.g., RF mixers. It is necessary to consider the enhanced parasitics.

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