Study on Compact Equivalent Circuit Model for RF CMOS Transistor

Rabnawaz Sarmad Uqaili, Faraz Bashir Soomro, Junaid Ahmed Uqaili, Ahsin Murtaza Bughio, Khalid Ali Khan

Abstract— In this study, a physical-based radio-frequency (RF) compact equivalent circuit model (CECM) for complementary metal-oxide-semiconductor (CMOS) transistor and its parameter extraction is presented. The whole structure of CECM that includes a small-signal equivalent circuit model of the transistor, a MOSFET small-signal substrate model, an input and output ground-signal-ground (GSG) pad model, a pad coupling model and a metal interconnection model are briefly studied and discussed. Based on this study, a complete test structure model for RF CMOS is designed and the initial values of parameters are extracted by using the analytical method. The multi-bias scattering parameters (S-Parameters) of model correspondence to the experimentation are validated up to 66 GHz and 220 GHz respectively. A good agreement has been achieved between the simulation and experimental under multi-bias conditions.

Index Terms— CMOS, equivalent circuit model, MOSFET, millimeter-wave, radio frequency, small-signal modeling, scattering parameters.

1 INTRODUCTION

THERE are some emerging challenges, along with the rapid development of applications in wireless communication [1]. The device scaling is directly responsible for Moore's law, and CMOS device has been significantly used for more than last 5 decades that has allowed to increase the number of transistors in chips with the extended multi-functions to enhance the performance of devices [2], [3]. Complementary metal-oxide-semiconductor (CMOS) transistor is the basic component of the integrated circuit (IC) design. Advanced CMOS technology is attractive to IC design because of its flexibility, availability, low cost and high integration [4], [5]. As the device size decreases, the channel resistance decreases, which in turn allows faster circuit operation. With the continuous improvement of intrinsic devices, parasitic components such as series resistance in source/drain regions begin to limit device performance. For this reason, the analysis of the CMOS model should be able to accurately predict the physical behavior of transistors [6], [8].

The accurate and exact measurement is the premise for RF CMOS modeling. The device under test (DUT) is not only part of the layout of the test structure but there are many parasitic structures in the layout. These parasitic effects of the structures in the model cannot be ignored for high-frequency devices. For this reason, the effects of parasitic structures can be removed from the device by using de-embedding techniques [9], [10], [11], [12], [13]. However, these effects at the high frequencies become very complicated. Therefore, it is not appropriate to obtain accurate data from the device by using de-embedding technology.

The suitable solution for this is to use analytical or equivalent circuit models (ECMs) that can characterize the effects of the parasitic structures. It is possible to have an equivalent circuit model that accounts for all the physical elements that are the part of RF CMOS transistor. However, it is always complex and hard to implement the model as compact for circuit simulations at very high frequencies. Many researchers in the literature have aimed to develop accurate and scalable models to support circuit design and to provide feedback for the fabrication process. The small-signal models have been extensively reported for the modeling of CMOS devices [14], [15], [16], [17], [18], [19]. The small signal-signal circuit model alone is not enough to accurately predict the behavior of the transistor over a wide frequency range. Therefore, a compact model is much needed that can serve as a link between the circuit design and process technology.

In [14], a scalable small-signal model is reported for the PHEMT transistor, however, the model was limited only to extrinsic parameters of the transistor. In [15], the small-signal model is reported that characterized the substrate-related parameters and their extraction. In [16], the RF CMOS model has been reported for characterizing the thermal noise for the substrate part. Gao et at. [17] presented a small signal model including the substrate part and extrinsic parameters are extracted against the device gate width. In 2010, Tang et at. [18] presented a new scalable small-signal model in which the coupling effects are described by using the gate-drain branch up to 40 GHz. In [19], the modeling of common source MOSFET fabricated in 65nm CMOS process is reported. In [20], a small signal model against 8 number of fingers was introduced and validated up to 66 GHz. However, in all the above-mentioned models, de-embedding technology is used to characterize the parasitic effects and de-embedded s-parameters are used to extract the parameters of the small-signal model. The existing modeling procedures are often insufficient to account for the rapid evolution of transistor technologies. Hence, transistor modeling is continuously the subject of intensive research, as novel methods are essentially required to model new transistors.

Under this scenario, the present work aims to provide an innovative compact equivalent circuit model that includes the small-signal model, MOSFET substrate model, input-output GSG pad model, improved pads coupling model and the metal interconnection model. This model can avoid the influence of improper de-embedding and provide a clear physical description of the entire test structure. All the parameters of the model are extracted and the entire CECM for RF CMOS is validated and verified with high accuracy

2 METHODOLOGY

2.1 Basic Component of the Model

The layout of the test structure is shown in fig. 1. The transmission lines interconnection connects the signal port from the GSG input-output pad to the MOSFET gate-drain. The corresponding wavelength decreases, as the operating frequency increases. Thus, the interconnections distributed parameter effects become more prominent. Furthermore, as the device is further scaled-down, the effects of metal stacking interconnection as well as the coupling between the top metal and substrate must be fully considered. In this regard, each parasitic structure is studied briefly to provide the physical meaning of the whole test structure.

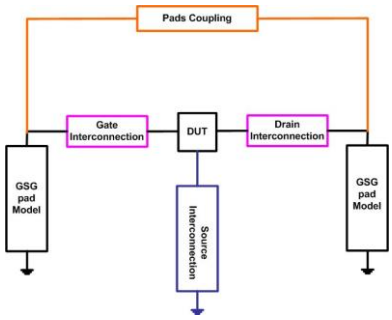

Fig. 1. Transistor Model with the test structure.

2.2 Small Signal Model for RF CMOS

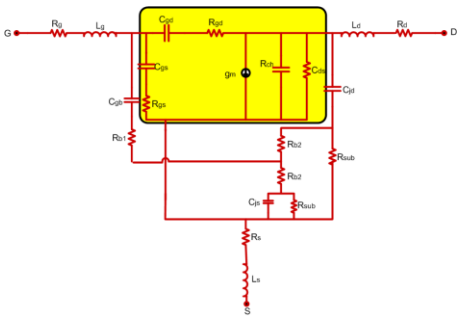

Fig. 2. Small-Signal Equivalent Circuit Model [20].

The small-signal model is shown in fig. 2, where R_g is the gate resistance, Rs is the transistor's source resistance. C_{gs}, C_{gd}, C_{ds} are the intrinsic capacitance, V_{gs} is the dependent current source, gm is the transconductance, R_{ds} is the channel length modulation effect, C_{sub} and R_{sub} are the substrate effect. R_g, R_s, R_d, C_{sub} and R_{sub} are parasitic parameters. These parameters are independent of bias and intrinsic parameters. In general, the substrate capacitance C_{sub} will vary with bias. At zero bias condition (V_{gs}=0 and V_{ds}=0).

2.3 MOSFET Small Signal Substrate Model

Fig. 3 shows the cross-sectional view of MOSFET and substrate of parasitic networks. The considerable ohmic loss, which is caused by the semiconductive silicon substrate, is characterized by R_{b1}, R_{b2} and R_{sub}. C_{js} and C_{jd} represent the junction capacitance of the source/drain region, C_{gb} represents the gate to substrate coupling capacitance and depletion layer capacitance. When the transistor operates at zero bias conditions (V_{gs}=0V & V_{ds}=0V), the nonlinear phenomenon of the phase of S_{11} and S_{22} can be observed. It significantly affects the transistor's state capacitance of the 'OFF' state and deepens the insertion loss and isolation for switch applications. Thus, the accuracy of the non-linear phase of S_{11} and S_{22} is necessary to consider. The new substrate model is established; this effect is characterized by a gate-drain substrate coupling network [23]. The substrate network with C_{gb} and C_{jd} characterizing the coupling path between gate and drain, thus, the equivalent circuit model of the CMOS transistor is applied with source and bulk connected.

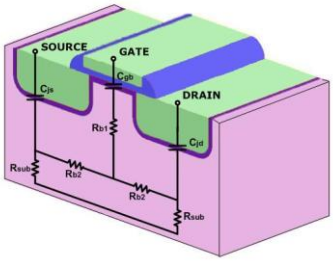

Fig. 3. Cross-Section View of MOSFET [23].

2.4 Input and output GSG pad Model

The cross-section view of GSG pad structure is shown in fig. 4. GSG pads are usually used for on-wafer testing in most RF IC designs. Precise compact models are therefore particularly valuable for efficient simulation for the design of the RF circuit. The S-pad is shielded by connecting the two G-pads using the bottom metal layer to reduce the loss caused by the silicon substrate.

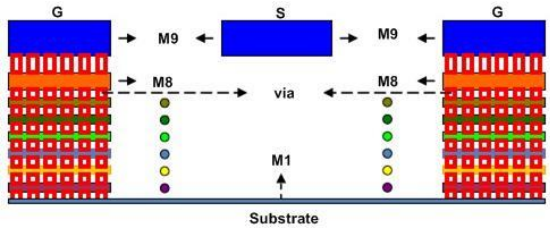

Fig. 4. GSG Pad Structure layout & cross-section view [24].

To obtain the individual parameter values, the circuit topology is simplified as shown in fig. 5, where M represents the coupling between the two inductors.

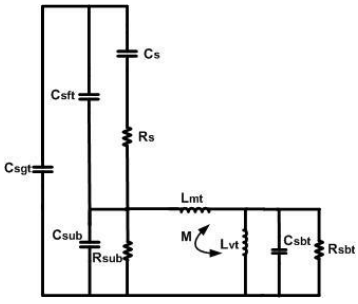

Fig. 5. Simplified GSG Pad Model.

2.5 Pad Coupling Model

In millimeter-wave frequency, as the device becomes more compact, the pad coupling will affect the transistor extensively. When frequency exceeds the 50 GHz, the input and output pads coupling effect becomes apparent. If this effect is not considered at this stage, it will lead to a significant deterioration in the accuracy of the model. So, when considering the extrinsic parasitic effects of the test structure, not only the GSG pad effect needs to be considered but the coupling of the input/output pads through the substrate also needs to be considered. The coupling of two GSG pads considered as a transmission path through the substrate has been reported [22]. There is a coupling path through the substrate between input and output pads, which can be represented by a compact model as shown in Fig. 6.

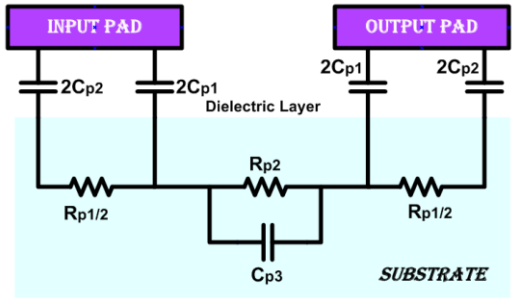

Fig. 6. Cross-Section View of MOSFET [23].

Each GSG pad has a distributed capacitance, (C_{p1}, R_{p1}, C_{p2}) which can be modeled by the RC network. R_{p2} and C_{p3} are used to model the coupling of the input/output pads through the substrate. This provides a simplified pad coupling circuit model. The parasitic effects of the test structure not only have the coupling of the input & output pads, but also include the interconnect effect, so when establishing the parasitic effect model for the test structure, it is necessary to establish an interconnection model.

2.6 Metal Interconnection Model

Interconnects are required to connect the pads. Therefore, in the entire model, the interconnection effect must also be considered. The transmission lines interconnection connects the signal port from the GSG input-output pad to the gate/drain of the MOSFET. First, the metal interconnects on the top layer can be simulated with a simple RL series structure; interconnects that are stacked from top to bottom layer can be molded with an inductor. Also, as the device is further scaled-down, the effects of metal stacking interconnection and the coupling between the top metal and substrate should be fully considered. However, due to the interconnection between the interconnect metal layer and the underlying metal layer, the coupling path is short and its dielectric loss is small enough to be ignored. So, for the simplicity of the model, the effect of dielectric loss is not considered in the branch. The simplified interconnection circuit model is shown in fig. 7.

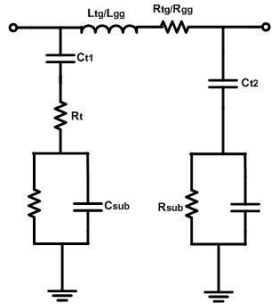

Fig. 7. Simplified Circuit Model of Interconnection [22].

3 ANALYSIS

On the basis of the MOSFET small-signal substrate model, the broadband input/output GSG pad model, pad coupling model and metal interconnection model; an improved compact equivalent circuit model for RF CMOS with the characteristics of all the parasitic effects is established as shown in Fig. 8.

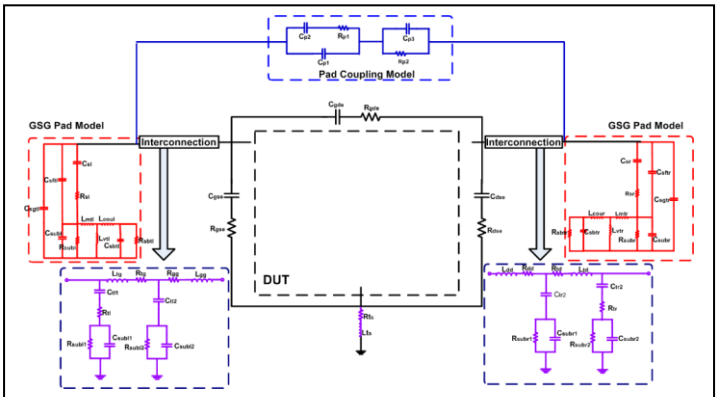

Fig. 8. The layout of the entire test structure.

In the input-output GSG pad model, the non-ideal fringe capacitance of the S-pad is represented by C_{sft} (C_{sftl}, C_{sftr}), and the capacitance and resistance of the lossy substrate are modeled at the bottom by paralleling C_{sub} and R_{sub} (C_{subl}, C_{subr} and R_{subl}, R_{subr}). The inductances of the stacked G-pad metal and the metal layer can be modeled by L_{vt} and L_{mt} (L_{vtl}, L_{vtr} and L_{mtl}, L_{mtr}). The parasitic resistance and capacitance between the S-pad and substrate can be modeled by R_{sbt} and C_{sbt} (R_{sbtl}, R_{sbtr} and C_{sbtl}, C_{sbtr}).

There is a coupling path through the substrate between input and output GSG pads which is characterized by the compact pad coupling model. Each pad is including a distributed capacitance which is represented by the lumped capacitances and resistance (C_{p1}, C_{p2}, R_{p1}) to avoid the effects of pad coupling that may affect the performance of the transistor. R_{p2} and C_{p3} can be used to model the coupling of the input/output pads through the substrate.

In the test structure, the GSG pad model and gate-drain of the device under test (DUT) are connected by the interconnection line. As the frequency increases causing the decreasing of the wavelength and in millimeter-wave frequency, the electrical length becomes shorter so the distributed parameters effects of

the metal interconnection model become very evident so it cannot be considered as the transmission line. In this regard, the metal stacking effects of the interconnection model and the effects of coupling between the metal and substrate are fully considered in the entire test structure. As shown in fig. 8, in the metal interconnection model, the coupling effect of gate and source, gate and drain, drain and source are modeled by C_{gse}, C_{gde}, C_{dse} and R_{gse}, R_{gde}, R_{dse} respectively. R_{tl}, R_{tr} and C_{tl1}, C_{tl2}, C_{tr1}, C_{tr2} describes the parasitic resistance and capacitance between the substrate and metal interconnection. The interconnection effects from source to the ground can be modeled by R_{ts} and L_{ts}. The gate-drain outgoing line in the metal of gate/drain is described by R_{gg}/L_{gg} and R_{dd}/L_{dd}. The transmission loss and phase shift from the pads to the gate-drain of the transistor is modeled by R_{tg}/L_{tg} and R_{td}/L_{td}.

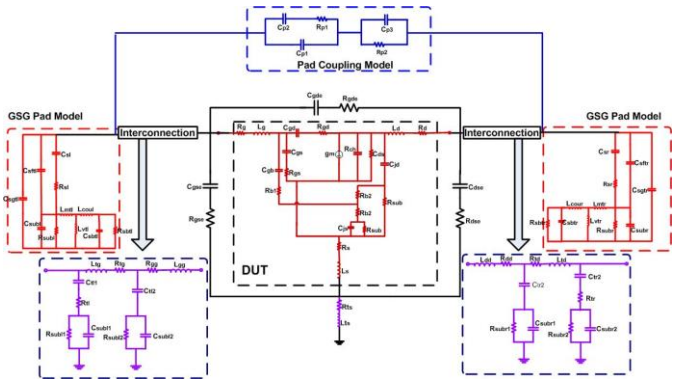

Fig. 9. Complete CECM for RF CMOS transistor with an entire test structure.

By introducing the small-signal model of RF CMOS in the test structure along with the substrate model, input-output GSG pad model, improved pads coupling model and the metal interconnection model, a complete test structure [21] is introduced in Fig. 9. The ohmic loss due to silicon substrate is characterized by a resistive network of R_{b2} and R_{sub}. The junction capacitance C_{jd} and C_{js} describes the drain to source/bulk signal coupling path. C_{gb} and R_{b1} model the effect of the depletion layer, gate oxide capacitance, and ohmic loss in the substrate coupling model. In the millimeter-wave range, the parasitic components at the gate due to the distributed transmission line and non-quasi-static effect (NQS) becomes prominent, it is characterized by R_{gs} and R_{gd} in series with C_{gs} and C_{gd}. The drain conductance of the channel is characterized by R_{ch} and gm is the transconductance. L_g, L_d, and L_s refer to the parasitic inductance, and R_g, R_d, and R_s refer to the parasitic resistance of the drain, gate, and source, respectively. The influences of maximum power transfers and noise figure can be characterized by R_g, however, R_g is a bias-independent component. The level of doping concentration is increased in a lightly doped drain, which can be model by bias-independent components i.e. R_d and R_s.

4 RESULTS AND DISCUSSIONS

To inspect the accuracy and for validation of the proposed model, the whole test structure of the transistor with a finger width of 650 nm is fabricated using a 90-nm RF CMOS technology with 32 number of fingers. S-parameters are obtained by an on-wafer measurement system. The test platform includes an Agilent network analyzer (E8461A), VNA frequency extenders (test heads) from Farran Technology, microwave probe stations (Summit 11000B-S, Cascade Microtech), probe platforms, and microscopes. The extracted parameters are obtained and optimized by the algorithm provided by the Advanced Design System (ADS) software. The simulated and experimental S-parameters in terms of the gate to source voltage V_{gs} and drain to source voltage V_{ds} are compared under multiple bias conditions as shown in fig 10 to 16. From fig. 10 to 14, a CECM is validated with higher accuracy up to 66 GHz under multi-bias conditions i.e. Bias 0 (V_{gs} = 0 V, V_{ds} = 0 V), Bias 1 (V_{gs} = 0.8 V, V_{ds} = 1.2 V), Bias 2 (V_{gs} = 0.9 V, V_{ds} = 1.5 V), Bias 3 (V_{gs} = 1 V, V_{ds} = 1 V), and Bias 4 (V_{gs} = 1 V, V_{ds} = 1.8 V). It is worth mentioning that the simulated results and measured results of CECM up to 220 GHz are not exactly the same in fig. 15 and 16. The main reason for the phase difference in S_{11} and S_{22} is an error in measurements, the higher the frequency, the more critical the measurement; which can be neglected at this stage. The model is very well suited for high frequencies. The extracted parameter values are in the acceptable range and physically realizable. The extracted component values of bias-dependent parameters are enlisted in Table-1. For verification purposes, root-mean-square error (RMSE) is calculated between the simulated and measured s-parameters. It depicts the error in S_{11} and S_{22} under 0.001 for all the bias conditions. High accuracy is achieved through RMSE for calculated and simulated results. Thus, CECM for RF CMOS is suitable for millimeter-wave RF circuits.

TABLE 1
EXTRACTED VALUES OF BIAS-DEPENDENT PARAMETERS OF CECM FOR RF CMOS

Components	Bias 0	Bias 1	Bias 2	Bias 3	Bias 4
R_{gd}, Ω	158.35	0.1	0.1	0.1	0.1
R_{gs}, Ω	435.1	114.14	114.5	10.38	107.9
R_{ch}, Ω	–	0.716	0.643	0.39	0.63
C_{gd}, *f*F	2.88	2.7	2.65	3.4	2.54
C_{gs}, *f*F	3.9	11.5	11.6	11.7	12.2
C_{ds}, *f*F	2.24	0.1	0.1	0.2	0.1
C_{jd}, *f*F	11.2	15.6	14.57	15.87	15.20
C_{gb}, *f*F	4.8	2.7	2.9	3.23	2.5
C_{js}, *f*F	9.23	16.4	18.6	20.6	17.5
G_m, *m*S	–	16.5	17.37	16.3	17.8

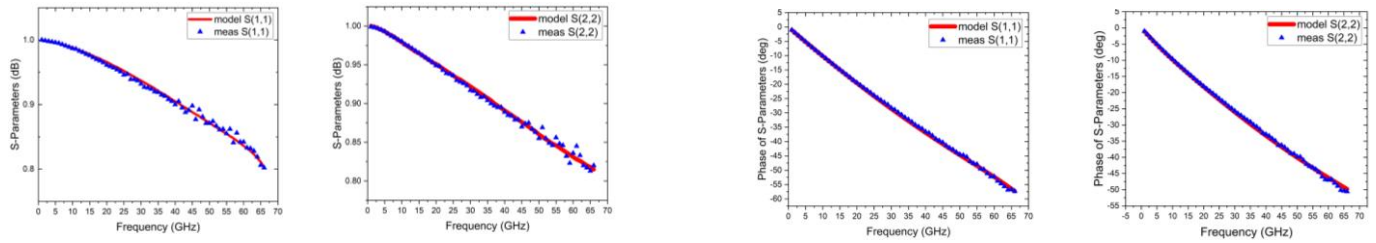

Fig. 10. Comparison between model simulated and measured results up to 66 GHz at Bias 0 (V_{gs}=0V & V_{ds}=0V).

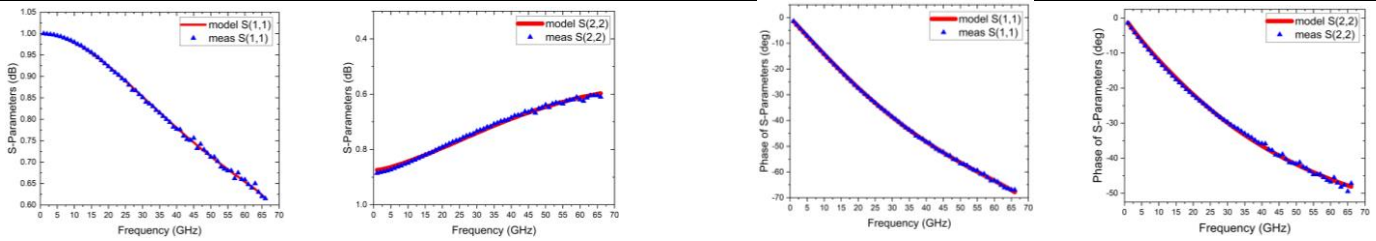

Fig. 11. Comparison between model simulated and measured results up to 66 GHz at Bias 1 (V_{gs}=0.8V & V_{ds}=1.2V).

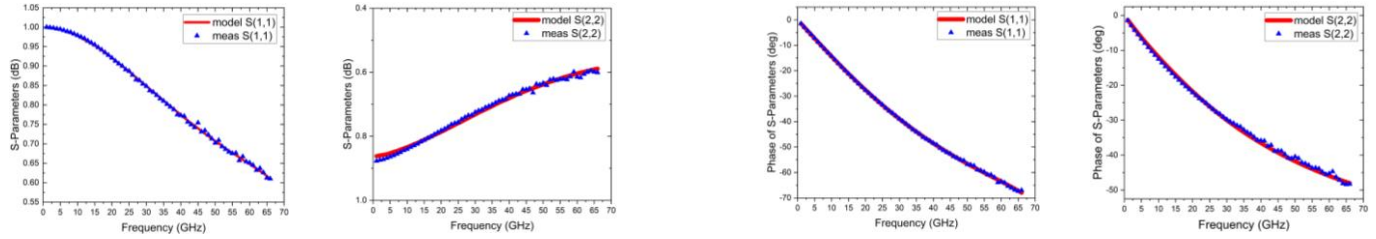

Fig. 12. Comparison between model simulated and measured results up to 66 GHz at Bias 2 (Vgs=0.9V & Vds=1.5V).

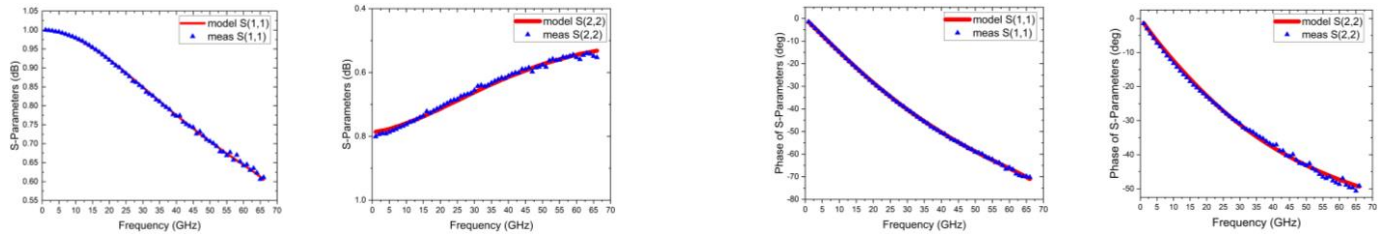

Fig. 13. Comparison between model simulated and measured results up to 66 GHz at Bias 3 (V_{gs}=1V & V_{ds}=1V).

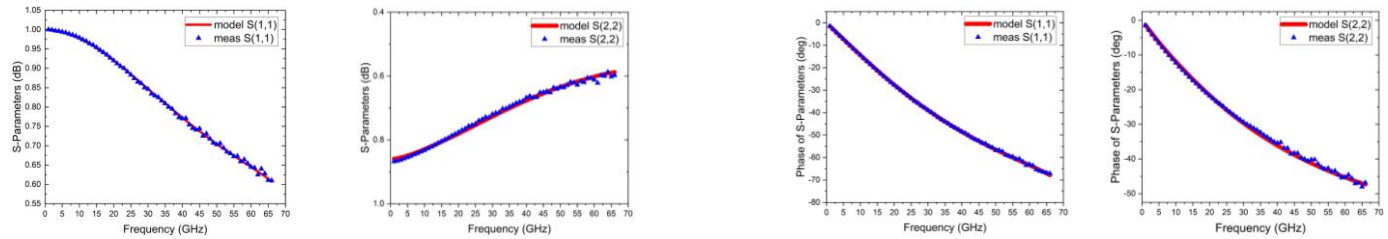

Fig. 14. Comparison between model simulated and measured results up to 66 GHz at Bias 4 (V_{gs}=1V & V_{ds}=1.8V).

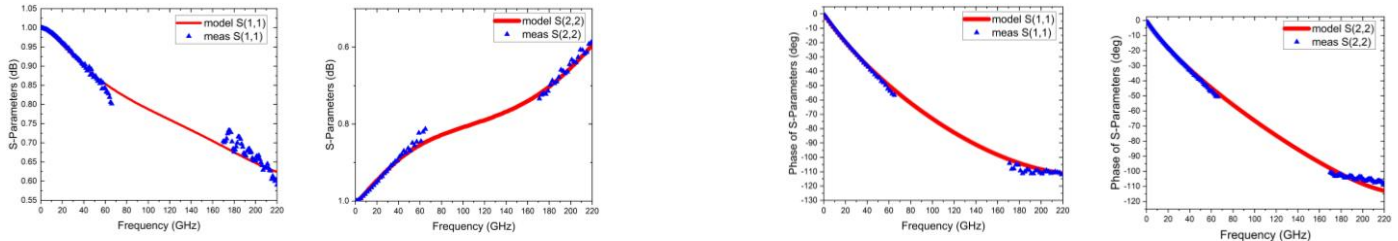

Fig. 15. Comparison between model simulated and measured results up to 220 GHz at Bias 0 (V_{gs}=0V & V_{ds}=0V).

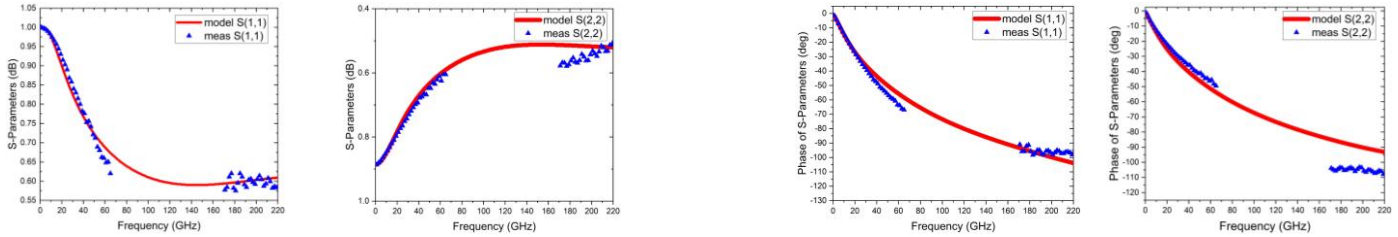

Fig. 16. Comparison between model simulated and measured results up to 220 GHz at Bias 1 (V_{gs}=0.8V & V_{ds}=1.2V).

5 CONCLUSION

In this work, the millimeter wave compact equivalent circuit model for RF CMOS transistor is established. In the entire test layout, the MOSFET substrate model, GSG input-output pad mode, pad coupling model and metal interconnection parasitics are fully characterized to avoid the domination of improper de-embedding. The component values of bias-dependent parameters are extracted through S-parameters. The model is validated and verified with high accuracy up to 66 GHz and 220 GHz respectively. The CECM is fabricated with 32 number of fingers using 90-nm CMOS process. The RMSE between the model simulated and the measured S-parameters are calculated under zero bias and active biases are within 0.0037 for S_{11} and 0.0042 for S_{22}.

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