Comparative Analysis Of Topologies Used In SEPIC Converter For Power Factor Correction

Pallavi M. Patode, Shrikant S. Mopari

Abstract: Expensive use of power electronic devices in various applications of power system which could result in power quality issues like low power factor, high THD, high electric stresses and complexity in cascaded connection. In order to overcome the above problems, there is a need to operate converter at unity power factor. In this work, a new modified multiplier SEPIC PFC topology is proposed and Comparative analysis has been carried out with conventional single stage SEPIC PFC topology. The performance of proposed topology can be Inspected by carrying simulation in MATLAB environment with PI and PID controller. The obtained results justice effectiveness of proposed work.

Index Terms: Conventional SEPIC PFC, Modified Multiplier SEPIC PFC, PI Controller, PID Controller

1. INTRODUCTION

With dc power requirements in electronic appliances, AC-DC converter becomes essential module for most of the power supplies. A diode bridge rectifier with output capacitive filter in this converter results in non-sinusoidal nature of source current with high THD. This causes low power factor and deteriorates power quality of utility system.[1] Concerning to enhance the power quality, topologies of AC-DC converter have been developed with active and passive PFC methods. In passive PFC only passive elements like capacitors and inductors are used to improve the nature of line current. While in active PFC, switching components with controller circuit are used to compensate distortion and displacement of input current waveform. As passive PFC methods result in lack of voltage regulation and poor dynamic response, more work has been done on active PFC methods. Buck, Boost, and Buck-Boost are the main active PFC topologies of AC-DC converter. Conventional Buck PFC topology maintains good efficiency for low power applications. Although when required output voltage is higher than input voltage it suffers from dead angle generation and can't keep harmonic standards [2]. Boost PFC is best alternative for such circumstances, however its use of high electrolytic capacitors after rectification results in distorted waveforms and reduction in efficiency [3]. In Buck-Boost PFC both lower and higher output voltage can be obtained, but has drawbacks like inverted output voltage and filter requirement at input and output side. A single ended primary inductance converter (SEPIC) is an AC-DC PFC converter which can provide noninverting output voltage with both higher and lower level than input voltage. Compared to other converters it has fast transient response, high-power density and good steady state performance. This advantages of SEPIC converter makes it more suitable over other converter for Power Factor Correction [4].In literature number of topologies are presented for SEPIC PFC. In paper [5] the author developed a single phase two switch SEPIC PFC topology which maintains input AC current sinusoidal and in phase with supply voltage with power factor of 0.99 and THD value below 5%. The author in paper [6] introduced a SEPIC PFC topology with active clamp circuit which have capability to reduce voltage stress by turning on ZVS (Zero Voltage Switching) of switch. Experimental result shows Power factor of 0.99 with 3.88% of THD. The author in paper [7] presented a multiplier approach in conventional SEPIC PFC which results in low switch voltage operation with 5.49% of THD and 0.99 of PF. By further modifying this topology, author [8] presented bridgeless configuration for modified multiplier topology. The drawback with bridgeless SEPIC topology is that, it includes two active switching devices which decreases overall accuracy of power stage and also increases overall cost of application. To reduce this drawback Author [9] presented a single switch bridgeless topology. This topology includes only one active switch and two additional diodes hence reduce overall cost of application. Experimental result shows 4.88% of THD with 0.998 Power Factor. However, this topology is applicable only for low power applications. For high voltage applications, coupled inductors and cascaded connection SEPIC topologies can achieve high voltage gain with some drawbacks such as complexity in circuit, increased number of switches and high voltage stress on switches. To overcome this drawback of cascaded connections, Author [10] presented a topology by considering both modified and multiplier topologies in SEPIC and proposed a 2x modified multiplier SEPIC PFC converter. This converter has only one active switch and high switching frequency which results in reduced voltage stress across switching device. High voltage gain, low current source THD values and Power factor near unity can be achieved for variable voltage range with this topology. Advantages of modified multiplier SEPIC PFC topology gives clear motivation to analyze this topology in more detail to clarify the operation and design of this concept with different controllers. This paper presents a comparative analysis of modified multiplier SEPIC PFC topology with conventional SEPIC PFC topology. Further the performance of proposed topology is evaluated with PI and PID controller for power factor and THD results.

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2 TOPOLOGY ANALYSIS

In this Part working operation of both topologies are presented and analyzed

2.1 CONVENTIONAL SINGLE STAGE SEPIC PFC TOPOLOGY:

Power circuit diagram of conventional single stage SEPIC PFC topology is as shown in fig.1. It consists of AC voltage input supply, bridge rectifier, Inductors L_1 and L_2, MOSFET as

switching device, capacitors C_1, C_2, with diode D and load resistance R.

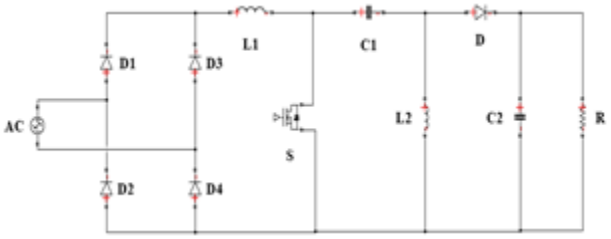

Fig.1 *conventional SEPIC PFC topology*

Regarding the 'ON' and 'OFF' condition of switching device, working of this topology separated in mode 1 and mode 2 operation as shown in Fig. 1.1 and Fig. 1.2 respectively. In mode 1 operation, switching device Q_1 turned on, diode D gets reverse biased and inductors L_1 starts to charge. Inductor L_2 and capacitor C_1 creates a resonant circuit and capacitor C_2 supplies current to the load. In mode 2 operation Q_1 turned off, and diode D gets forward biased.L_1-C_1-L_2 creates a loop. The load gets directly connected to the inductors which result in discharge of inductors.

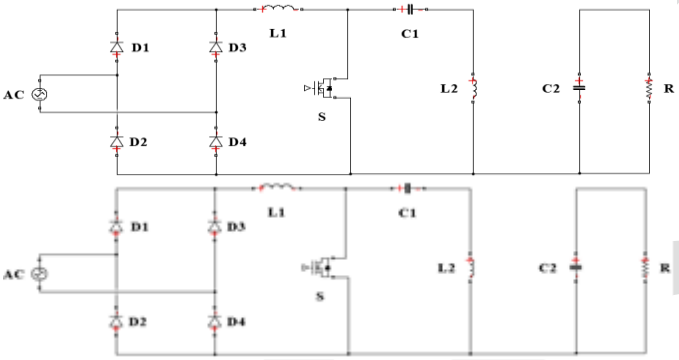

Fig.1.*1 Switch ON mode of conventional SEPIC PFC topology*

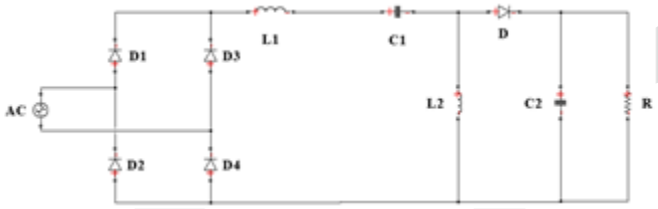

Fig.1.2 *Switch OFF mode of conventional SEPIC PFC topology*

2.2 MODIFIED MULTIPLIER SEPIC PFC TOPOLOGY:

This topology is designed by merging multiplier SEPIC topology and modified SEPIC topology with the purpose of achieving high voltage output. Fig.2 shows the circuit diagram for Modified multiplier SEPIC PFC topology. It contains AC voltage supply with diode bridge rectifier, diodes D_1,D_2,D_3,D_m and capacitors C_1,C_2,C_3,C_S,C_m. One Switching device and resistance R as a load.

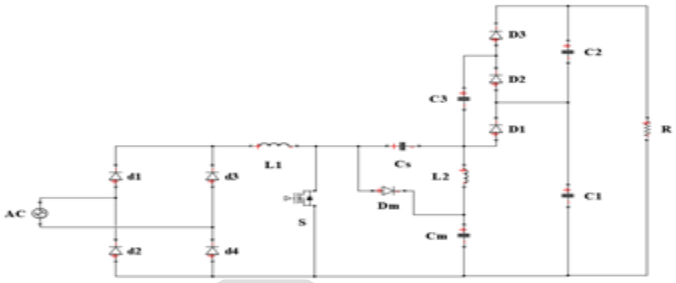

Fig.2 *Modified Multiplier SEPIC PFC topology*

Working of modified multiplier SEPIC PFC is also a two-mode operation regarding 'ON' and 'OFF' condition of switching device as shown in the fig.2.1 and Fig.2.2. respectively. In mode 1, when switch Q_1 is turned ON, inductor L_1 starts to store energy from supply voltage while inductor L_2 store it from capacitors Cm and Cs. Diodes D_1, Dm, D_3 get reverse biased. Capacitor C_1 transfers energy to capacitor C_3 through diode D_2 and the load is supplied by capacitor C_2 only. In mode 2 operation, switch Q_1 turned off, Diode Dm, D_1, D_3 get forward biased and D_2 gets reverse biased. Capacitors Cs and Cm get charged by stored energy of inductor L_1. In this duration voltage across the switch (V_Q) is same as that of voltage across capacitor Cm (Vc_m). capacitor C_1 gets charged by inductor L_2 through diode D_1. capacitor C_2 gets charged by energy transfer from capacitor C_3 through diode D_3. hence load is supplied by C_1 and C_2 which result in increased voltage gain without rise in duty ratio.

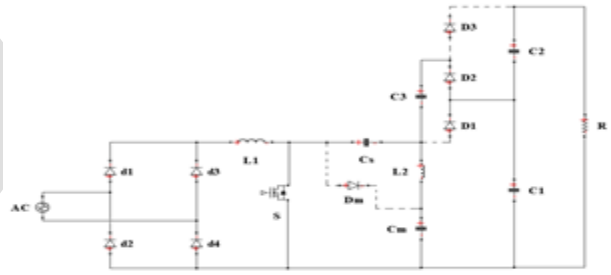

Fig.2.1 *Switch ON mode of modified multiplier SEPIC PFC topology*

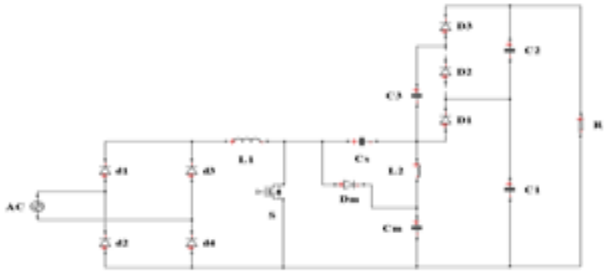

Fig.2.2 *Switch OFF mode of Modified multiplier SEPIC PFC topology*

3 TOPOLOGY DESIGN

With the reference of paper [13], output voltage for proposed modified multiplier SEPIC PFC converter is given as,

$$V_o = V_{in}\left(\frac{2+D}{1-D}\right) \quad (1)$$

Inductor value L is given as,

$$L = \frac{V_{in} \times D}{2\Delta_{Il} \times F_{sw}} \quad (2)$$

Coupling Capacitors Cs and Cm is given as,

$$C = \frac{I_{out}}{\Delta V \times F_{sw}} \quad (3)$$

(Here C=Cm= Cs)

Value of output capacitors is calculated as,

$$C_f = \frac{C_1 C_2}{(C_1 + C_2)} \quad (4)$$

(Here C1=C2=C3)

And

$$C_f \geq \frac{P_o}{2\pi F_{ac} V_o \Delta V_o}$$

With this prototype, the calculated design parameters for this topology is given in table 1. for this topology, input AC voltage is given as 230V, rated resistive load is taken as 1600 Ohms and switching frequency is selected as 50kHz.

TABLE 1
Design parameters

Parameters	Values
Capacitor Cm and Cs	1µF
Inductor L_2 and L_1	0.98 mH
Capacitor C_1, C_2, C_3	590µF
Switching frequency	50 kHz
Input voltage (AC)	230 V

4 CONTROL CIRCUIT

Performance analysis of proposed topology is examined with two different control systems, first is PWM control technique [11] with PI Controller and second one is Multi Loop control system [9] with PID Controller. Fig.3 shows the block diagram of PWM control system with Discrete PI controller. In this system output dc voltage is compared with constant voltage reference value. The obtained signal from the comparison is given as error signal for PI controller. PI controller reduces the error of signal and adjusted the signal to minimize phase shift between voltage and current to obtain power factor near unity. The signal is further passed throw relational operator where it gets compared with repeating sequence waveform to convert the signal into desirable waveform

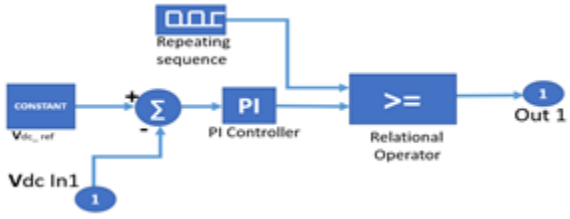

Fig.3 *Subsystem of PI Controller*

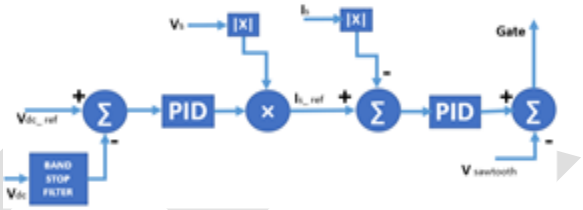

Fig.4 *Subsystem of PID Controller*

Fig.4 shows the block diagram for PID Controller with Multi Loop control system. for this control system, measured dc voltage is passed throw Band Stop Filter to reduce noise in the measurement and then compared with the constant value of reference dc voltage. The value of constant is taken as per requirement of Output dc voltage by the user. The error signal obtained is then given to first PID controller which works as a Voltage Controller to minimize the error in signal. This signal is further multiplied with the source voltage to generate reference current which regulate dc voltage. This signal is again compared with the source current to generate error signal and fed to second PID controller which minimize the error. Further, this signal is compared with sawtooth waveform to generate gate signal for switching device.

5 SIMULATION RESULTS

In this section, the MATLAB Simulation performance of the modified multiplier SEPIC PFC topologies with PI and PID controller are evaluated and compared to the MATLAB Simulation performance of conventional SEPIC PFC topology. For this, all these topologies are provided with same input power supply. Fig.5 shows input current and voltage waveform for conventional SEPIC PFC topology. The measured power factor for this topology is 0.9678

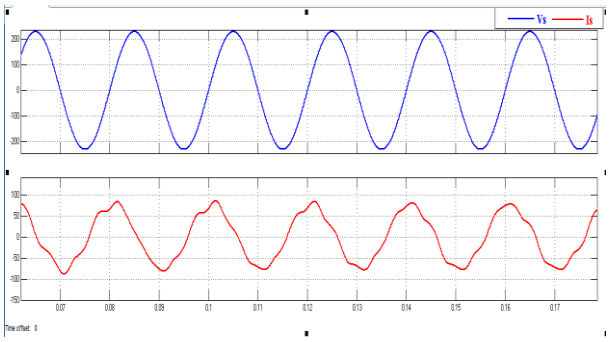

Fig.5 *Input voltage and current waveform for conventional SEPIC PFC topology with PI controller*

From Fig.5, it is observed that for conventional SEPIC PFC topology, the input current waveform is distorted and not in phase with input voltage waveform. With PI controller, the measured input current THD value is 11.50%. Fig.6 shows FFT Analysis for conventional SEPIC PFC topology.

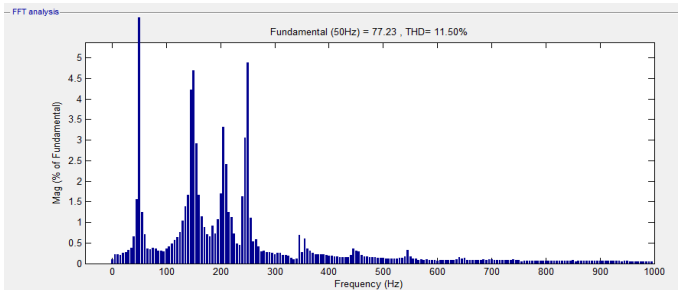

Fig.6 *FFT analysis of Conventional SEPIC PFC topology with PI controller*

Fig.7 shows output waveforms of Conventional SEPIC PFC topology with PI controller for voltage and current.

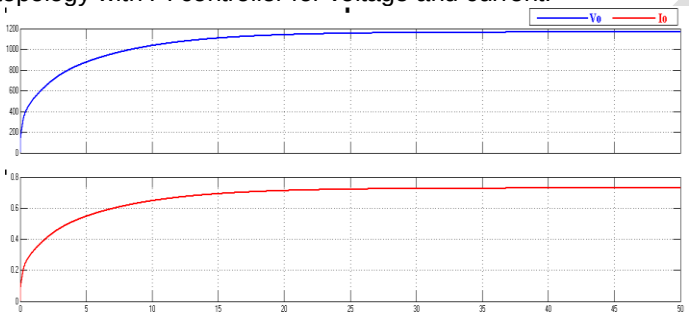

Fig.7 *Output voltage and current waveform for conventional SEPIC PFC topology with PI controller*

Fig.8 and Fig.9 shows Modified multiplier SEPIC PFC topology with PI controller input output waveforms for voltage and current. Fig 10 shows FFT analysis for the same. the measured PF for this topology is 0.98 for full load.

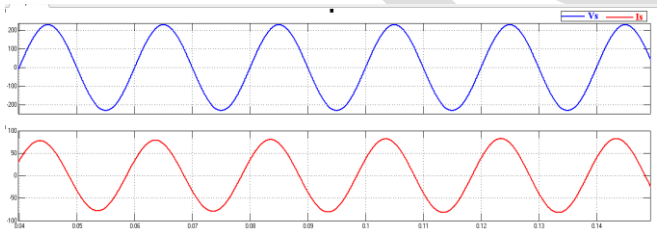

Fig.8 *Input voltage and current waveform for Modified multiplier SEPIC PFC topology with PI controller*

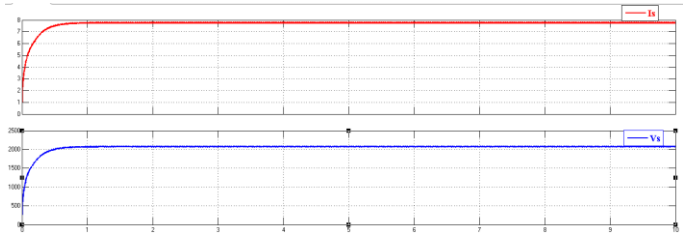

Fig.9 *Output current and voltage waveform for Modified multiplier SEPIC PFC topology with PI controller*

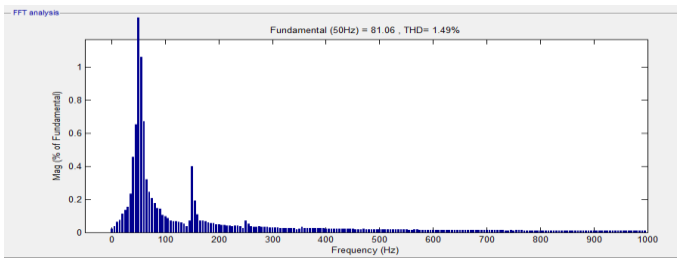

Fig.10 *FFT analysis for Modified multiplier SEPIC PFC topology with PI controller*

From the input, output waveforms of Modified multiplier SEPIC PFC topology with PI controller, it is observed that the value of THD in source current get reduced significantly, also PF get improved up to 0.9867 for full load condition. Simulation results for this topology with PID controller are represented in fig.11 and fig.12 for input and output voltage-current waveforms respectively and fig.13 shows FFT analysis for the same. From the waveforms, it is observed that with this topology, results get further improved for Modified multiplier SEPIC PFC compared to with PI controller. For this topology, value of THD is 0.06% and that of PF is 0.9928.

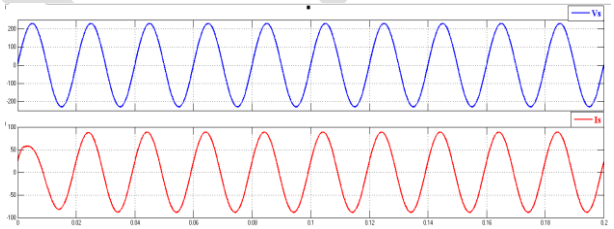

Fig.11 *input voltage and current waveform for Modified multiplier SEPIC PFC topology with PID controller*

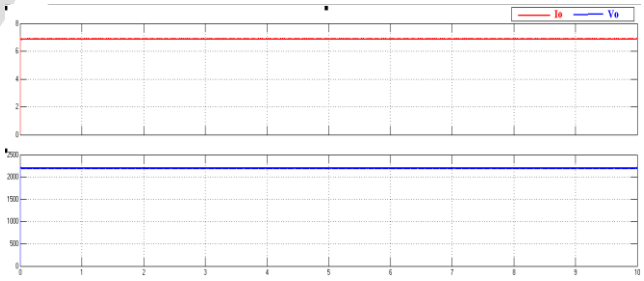

Fig.12 *output current and voltage waveform for Modified multiplier SEPIC PFC topology with PID controller*

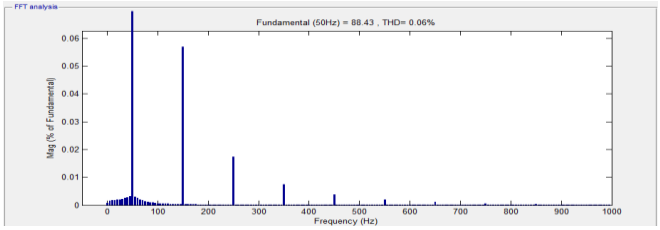

Fig.13 *FFT analysis for Modified multiplier SEPIC PFC topology with PID controller*

A comparative performance analysis of these topologies is presented in table 2

TABLE.2

COMPARATIVE ANALYSIS OF TOPOLOGIES

Topology	Source current THD	Power Factor
Conventional SEPIC topology	11.50%	0.9678
Modified multiplier SEPIC with PI controller	1.75%	0.9867
Modified multiplier SEPIC with PID controller	0.06%	0.9928

From table 2. It is observed that, compared to conventional SEPIC PFC topology, Modified multiplier SEPIC PFC topology with both PI and PID controller have good results for current source THD and PF improvement. Further comparison of performance of Modified multiplier SEPIC PFC topology for different rating of load with PI and PID controller is represented in table 3.

TABLE.3

POWER QUALITY INDICES OF MODIFIED MULTIPLIER TOPOLOGY FOR VARIABLE LOAD CONDITIONS

LOAD	WITH PI CONTROLLER		WITH PID CONTROLLER	
	THD	PF	THD	PF
100%	1.49	0.9867	0.06	0.9928
90%	1.52	0.9867	0.07	0.9928
80%	1.54	0.9867	0.07	0.9928
70%	1.59	0.9867	0.08	0.9928
60%	1.64	0.9867	0.10	0.9928
50%	1.75	0.9867	0.12	0.9928
40%	1.74	0.9867	0.14	0.9928
30%	1.30	0.9871	0.19	0.9928
20%	0.58	0.9879	0.28	0.9928
10%	0.22	0.9879	0.53	0.9928

6 CONCLUSION

In this work, a new Modified multiplier SEPIC PFC topology is analyzed with PI and PID controller. To validate its performance and power quality enhancement, The comparative analysis has been carried out between conventional SEPIC topology and modified multiplier SEPIC with PI and PID controller. PF up to 0.9678 and reduction in THD of source current up to 11.50% has been obtained with conventional SEPIC PFC topology. Whereas with Modified multiplier SEPIC PFC topology, PF gets improved up to 0.9867 and THD get reduced up to 1.49% for full load condition. the same topology with PID controller can improve PF up to 0.9928 and reduce THD up to 0.06%.Thus, Modified multiplier topologies with both PI and PID controller has shown better results for power quality improvement than the conventional SEPIC PFC topology. The proposed new Modified multiplier with PID controller topology is validated under variable load conditions and shown better performance.

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