# Comparison Analysis Of N-Channel And P-Channel SOI / Bulk Finfets

**V Vijayalakshmi, Dr. B. Mohan Kumar Naik**

**Abstract**: In this research paper, a 3 dimensional device simulation of 20 nm n-channel and p-channel SOI FinFET and Bulk FinFET have been studied. The electrical parameters such as electrostatic potential, electric field, current density, transfer characteristics, output characteristics, drive current, OFF state current and transconductance are investigated based on the various bias voltages. The transfer characteristics of SOI FinFETs are compared with that of bulk FinFETs. Based on the comparison analysis SOI FinFETs are more dominant over bulk FinFETs because of large $I_{ON}/I_{OFF}$ ratio in wide circuit applications and semiconductor memories.

**Index Terms**: nFinFET, pFinFET, SOI FinFET, Bulk FinFET, Drain Current.

## 1. INTRODUCTION

In this demanding VLSI Industry semiconductor memory plays a major role and occupies a large chip area in many of the VLSI circuit design [1-3]. As memory consumes a large fraction of many future designs, scaling of the memory density must continue to track the scaling trends of logic In the past few decades semiconductor industry is emerging with development of novel devices since Conventional Metal Oxide Semiconductor Field Effect Transistor (MOSFET) as a device in deepsubmicron technology node, suffers from short channel effects such as Drain Induced Barrier Lowering (DIBL), hot electron effects etc. Researchers find that leakage currents can be reduced by employing new device structures such as FinFET (Fin Field Effect Transistors) and TFET (Tunnel Field Effect Transistors). The complementary Metal Oxide Semiconductors technology node is shrinking, resulting in accumulating billions of transistors in a single chip. The necessity for ultra low power design thus keeps increasing. To cater this challenge more non conventional devices are developed for complex and portable circuits with low power consumption and greater efficiency [4-7]. To reduce both static and dynamic power in the circuit the device is miniaturized and reducing the operating voltages which increases the delay of the circuit and degrades the performance of the circuit [8,9]. Despite the fact that TFET has less leakage current, it has smaller ON current than FinFET. To increase the ON current, a strong electric field is to be applied at the tunneling junction. A high gate voltage is to be applied powerVLSI circuits for a strong electric field; however this results in increased power consumption in TFETs. Hence, FinFET remains the desirable choice for researchers for the design of low power VLSI circuits[10-13].In this article, the comparison analysis is carried out for bulk FinFET and SOI FinFET by considering both nFinFET and pFinFET. In section 2 the device structure is explained for both Bulk and SOI FinFETs. In section 3, the electrical characteristics for respective devices are discussed and analyzed. In section 4 the results are concluded.


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## 2 DEVICE STRUCTURE

Three dimensional structure for bulk FinFET and SOI FinFET are shown in figure 1(a) and (b)

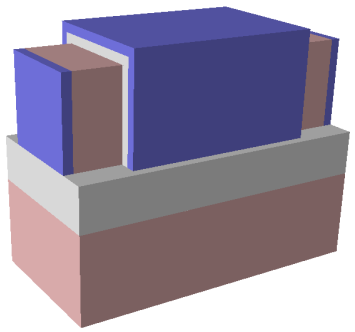

***Figure 1(a)****3D BULK FinFET*

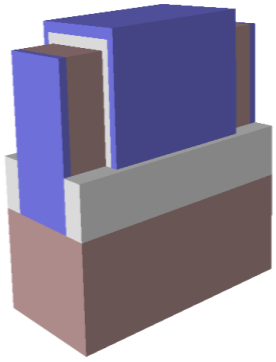

***Figure 1(b)****3D SOI FinFET*

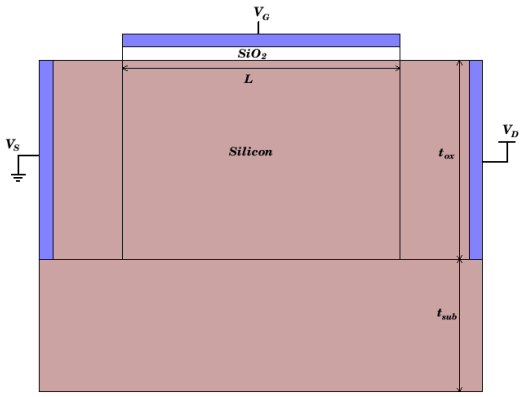


***Figure 1 (a)*** *2D cross section of bulk FinFET*

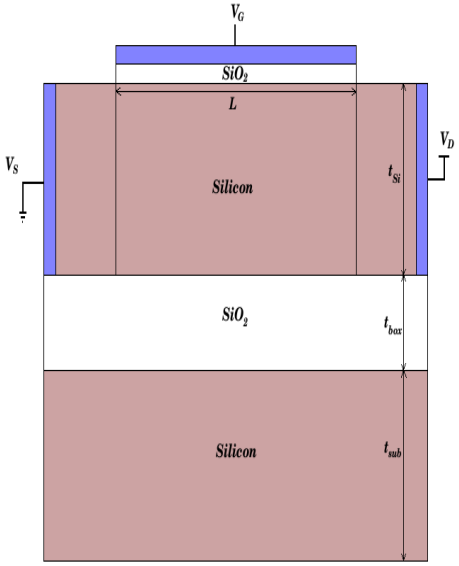


***Figure 2 (b)*** *2D cross section of SOI FinFET*

***Table 1*** *Device Parameters for nFinFET and pFinFET*

| Sl. No. | Device Parameter | Values for SOI FinFET | Values for Bulk FinFET |
|---|---|---|---|
| 1. | Channel Length (L) | 20 nm | 20 nm |
| 2. | Channel Width (W) | 10 nm | 10 nm |
| 3. | Channel Height (H) | 12 nm | 12 nm |
| 4. | Source and Drain Doping Concentration ($N_S$ & $N_D$) | $10^{19}$ $cm^{-3}$ | $10^{19}$ $cm^{-3}$ |
| 5. | Channel Doping Concentration ($N_C$) | $10^{18}$ $cm^{-3}$ | $10^{18}$ $cm^{-3}$ |
| 6. | Buried Oxide thickness ($t_{box}$) | 10 nm | - |
| 7. | Substrate Thickness ($t_{sub}$) | 10 nm | 10 nm |
| 8. | Oxide Thickness ($t_{ox}$) | 1 nm | 1 nm |

and Similarly 2 D cross section of respective devices are shown in figure 2(a) and (b) respectively, where L, W, H, $t_{ox}$ and $t_{box}$ are the Length, Width and Height of the channel, thickness of oxide layer and buried oxide layer respectively. It has been assumed that the FinFET is operated in the sub threshold region where mobile carriers are neglected and source to channel & drain to channel region jumps are abrupt. Table 1shows all the device parameters of Tri-gate FinFETs. All the device parameters are listed in table 1.

## 3 RESULTS AND DISCUSSIONS

In this section, we present the 3D TCAD simulation results of electrical parameters of n channel and p channel bulk and SOI FinFET. The device simulations of both the structures are carried out using TCAD tool. The simulation is performed by considering the physical models including SRH, CVT and BGN.

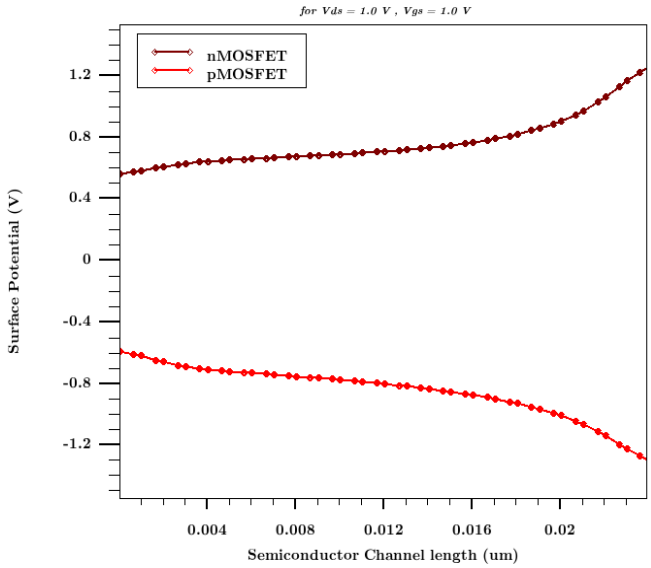


***Figure 3*** *Surface Potential Plot for n channel and p channel Bulk FinFET Device*

Schockley–Read–Hall (SRH) is a recombination model, which is used to characterize the device at high current densities and model the recombination through defects, respectively. The band gap narrowing model (BGN) was implemented to consider the high doping concentration in the substrate and source region. The CVT mobility model is used which activates velocity saturation effect and throughout the simulation a default thermal boundary 300 K is used [14]. Figure 3 shows the plot for surface potential for both n channel and p channel bulk FinFET along the channel length with input gate bias $V_{GS}$=1 V a constant drain bias $V_{DS}$=1 V. based on the above figure it is clearly seen that surface potential is dependent on majority charge carriers in both n channel (electrons) and p channel (holes) bulk FinFET. Surface potential of n channel device increases along with the channel length thus providing a thicker inversion charge layer for electrons to migrate from source to drain along the channel of the device.

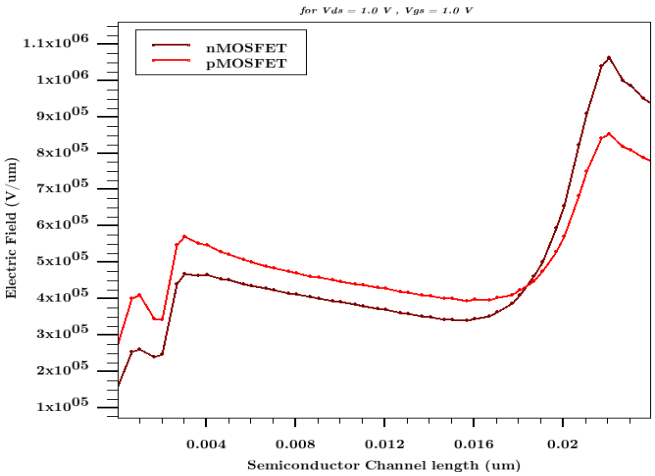


***Figure 4*** *Total Electric Field for n channel and p channel Bulk FinFET*

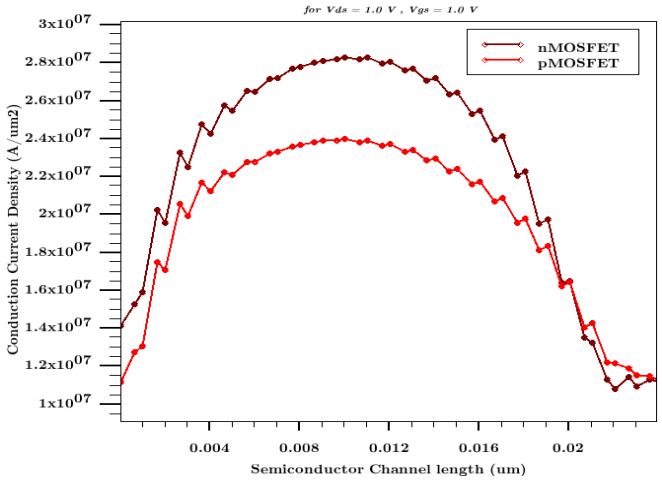


***Figure 5*** *Conduction Current Density for n channel and p channel bulk FinFET*

Figure 4 shows the plot of total electric field along the channel length for with input gate bias $V_{GS}$=1 V a constant drain bias $V_{DS}$=1 V. the plot shows the variation in electric field along the source-channel and channel-drain junction which increases along with channel length being a dependent parameter of surface potential. Electric Field for n channel device is higher than the p channel device due to more number of electrons.

***Figure*** *5 deploys the conduction current density plot for both n channel and p channel FinFETs.*

Conduction current arises when there are free electrons in a substance that are not too rigidly bound to the atom. The total amount of charge passing a point per second per unit area is then the conduction current density. The above figure shows the current density is more for n channel device.

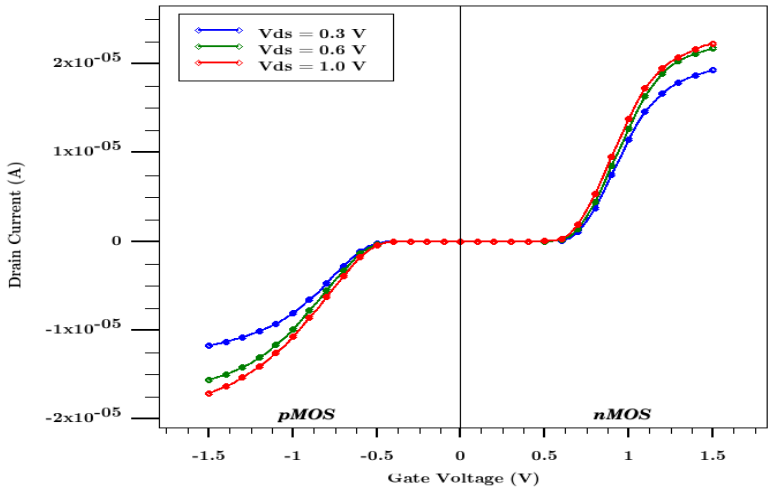


***Figure 6.a*** *Transfer Characteristics for n channel and p channel Bulk FinFET device*

Figure 6 shows the V-I characteristics in both linear and logarithmic scale for different drain biases, linear part of V-I characteristics (figure 6.a) shows the higher value of drain current for higher input drain bias for n channel bulk FinFETs and lower for lower drain bias for p channel FinFET, which also shows the on current variation along with the input biases.

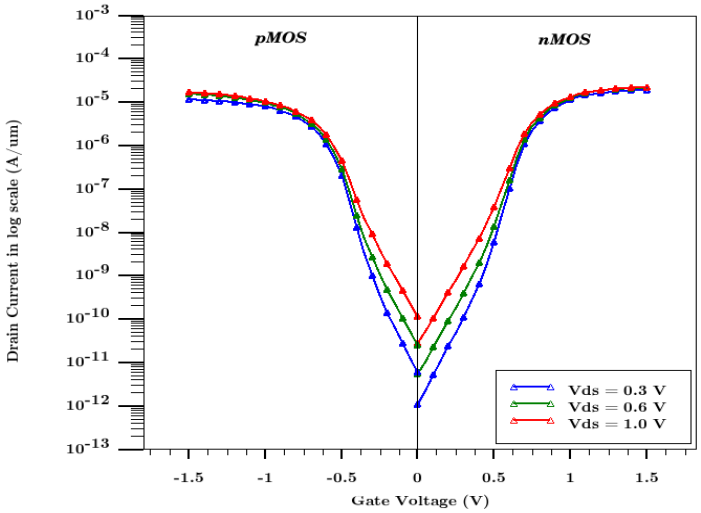


***Figure 6.b*** *Transfer Characteristics for n channel and p channel Bulk FinFET device in logarithmic scale*

Logarithmic scale of V-I characteristics (figure 6.b) shows the off current ($I_{OFF}$) as well as on current ($I_{ON}$) of the device. The performance of the device is gauged by the higher $I_{ON}/I_{OFF}$ ratio. Bulk FinFET shows an OFF current of $10^{-12}$ A and ON current of $10^{-5}$ A with $I_{ON}/I_{OFF}$ ratio of around $10^{7}$ for drain bias of 0.6 V.

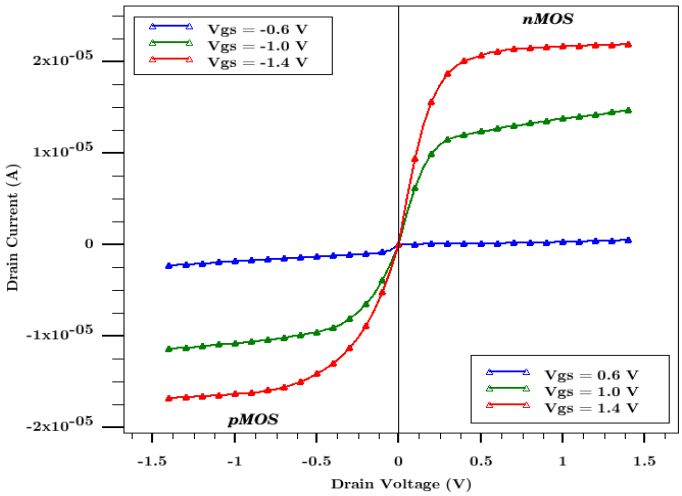


***Figure 7*** *Output Characteristics for n channel and p channel bulk FinFET*

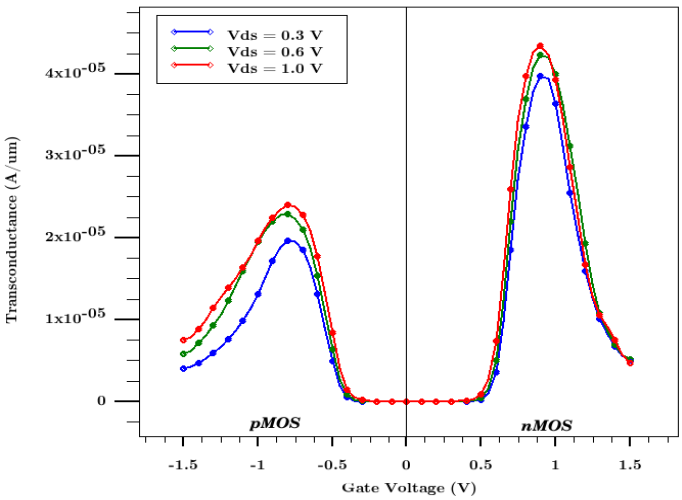


***Figure 3*** *Transconductance for n channel and p channel bulk FinFET*

Fig 7 shows the plot for output characteristics for n channel and p channel bulk FinFET for varied input gate bias. It shows no current for the input gate (0.6 V) to source voltage less than threshold voltage (0.62 V). It shows constant drain current for input voltage less than 1.4 V, after reaching the saturation point for drain saturation voltage $V_{DSat}$. For the input voltage above 1.4 V the channel undergo channel length modulation and with effect to this output current starts increasing linearly with respect to drain bias.

Fig 8 shows the AC parameter such as Transconductance for n channel and p channel Tri-gate FinFET. Transconductance shows the sensitivity of the device i.e., for a small change in input gate voltage how the subthreshold current varies in the device.

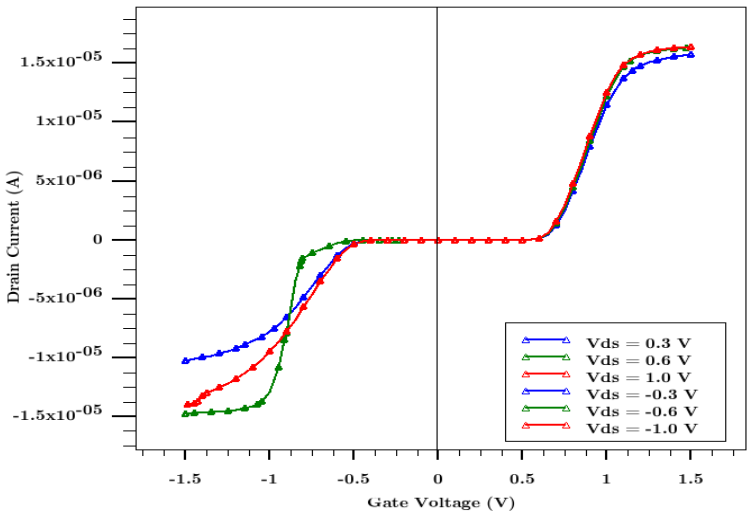


***Figure 4.a*** *Transfer characteristics for n channel and p channel SOI FinFET*

Similar to the transfer characteristics for bulk FinFET which was discussed in figure 6, Figure 9 shows the V-I characteristics for n channel and p channel SOI FinFET. Figure 9.b shows the logarithmic plot for subthreshold current which results in OFF current of $10^{-16}$ A for n channel and $10^{-14}$ A for p channel SOI FinFETs and with ON current of $10^{-5}$ A for both n channel and p channel device and shows a ION/IOFF ratio of $10^{11}$ for n channel and $10^{9}$ for p channel devices.

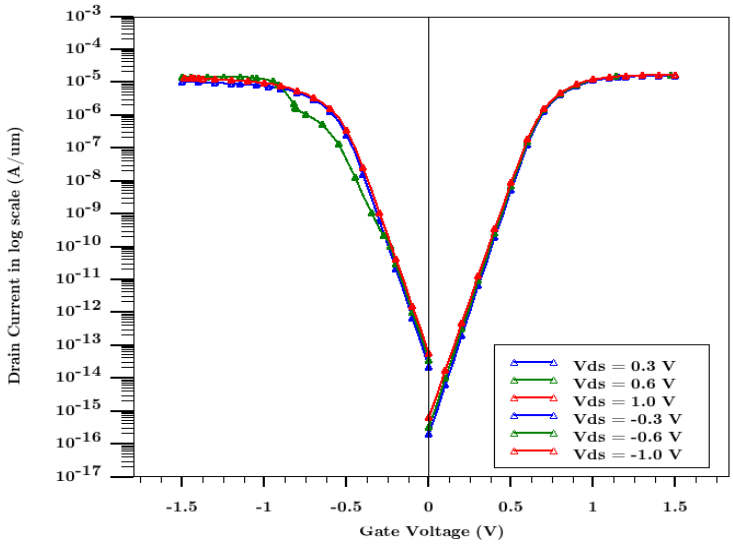


***Figure 9.b*** *Transfer characteristics for n channel and p channel SOI FinFET in logarithmic scale*

Figure 10 shows the output characteristics for n channel and p channel SOI FinFETs as discussed in figure 7 it shows a better performance for higher gate bias.

Figure 11 shows the comparison plot for subthreshold current for both bulk and SOI FinFETs. The analysis is carried for n channel and p channel devices. It clearly shows that SOI devices show a higher $I_{ON}/I_{OFF}$ of $10^{11}$ for n channel and $10^{9}$ for p channel devices. Meanwhile bulk device shows an $I_{ON}/I_{OFF}$ of $10^{7}$ for n channel and $10^{5}$ for p channel devices. Thus SOI devices shows higher switching speed (due to higher $I_{ON}/I_{OFF}$) and low power dissipation (due to lower $I_{OFF}$) for circuit application.

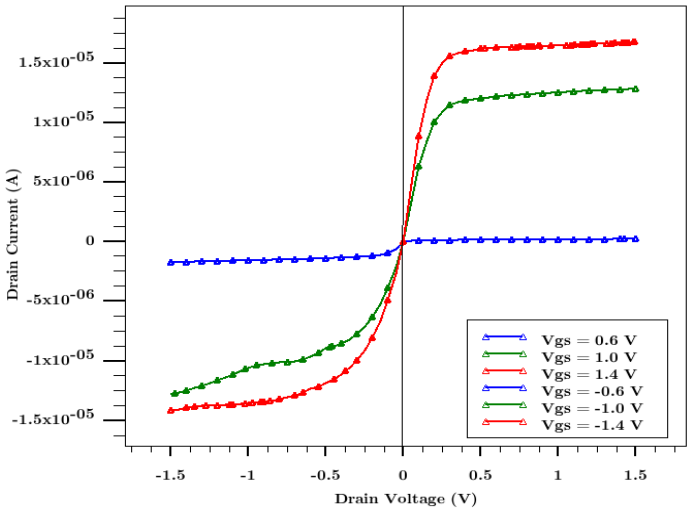


***Figure 5*** *Output Characteristics for n channel and p channel SOI FinFET*

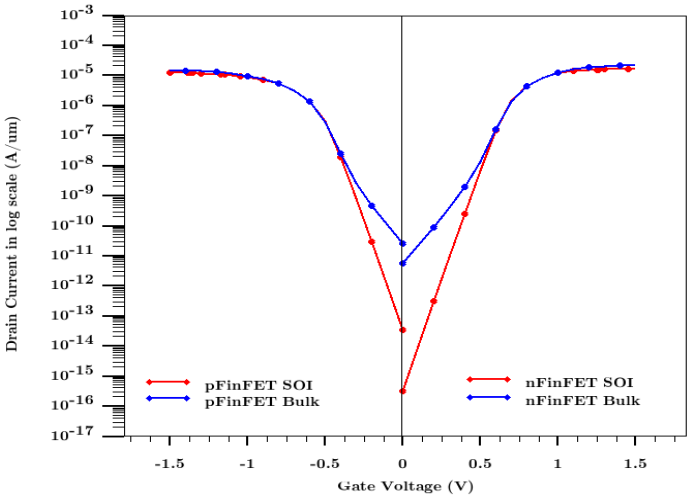


***Figure 11*** *Comparison plot for subthreshold current of n channel and p channel for bulk and SOI FinFET device*

## 4 CONCLUSION

The 3 dimensional device simulations of 20 nm n-channel and p-channel SOI FinFET and Bulk FinFET have been discussed. The electrical parameters such as electrostatic potential, electric field, current density, transfer characteristics, output characteristics, drive current, OFF state current and transconductance are investigated based on the various bias voltages. The transfer characteristics of SOI FinFETs are compared with that of bulk FinFETs. Based on the comparison analysis SOI FinFETs are more dominant over bulk FinFETs because of higher $I_{ON}/I_{OFF}$ ratio of $10^{11}$ for n channel and $10^{9}$ for p channel device, thus being an ideal device for circut applicatons and semiconductor memories.

## ACKNOWLEDGMENT

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