Design And Analysis of Clocked Subsystem Elements Using Leakage Reduction Technique

Sanjay Singh, S.K. Singh, Mahesh Kumar Singh, Raj Kumar Sagar

Abstract— As the density and operating speed of CMOS VLSI chips increases, leakage power dissipation becomes more and more significant. This paper presents a leakage power behavior in Pulse triggered flip-flop. All the designs are simulated with and without the application of leakage reduction techniques and the readings are presented. By analyzing the leakage path of flip flops we propose a method to reduce the leakage power of flip flops in this paper. The circuit are simulated using TANNER Tool SPICE simulator. The result at a frequency of 400MHz shows that proposed Flip-flop consume less power.

Index Terms— Flip-flop, leakage power, stack transistor and pulse generator..

1 INTRODUCTION

With the scaling of CMOS technology, leakage power is expected to become a significant portion of total power consumption in future CMOS system. To minimize the power consumption and to increase the battery life time, the supply voltage Vdd has been scaled down continuously. But the propagation delay Tpd of a circuit is inversely proportional to the square of the difference between the supply voltage Vdd and the threshold voltage Vt of the transistors. So scaling down the supply voltage, without scaling down the threshold voltage increases the propagation delay. However the threshold voltage scaling results in substantial increase of sub-threshold leakage current, which increases the leakage or static power dissipation of the VLSI circuits [1]. Leakage power dissipation is the power dissipated by the circuit when it is in sleep mode or standby mode.

$$Pleak = Ileak * Vdd \quad (1)$$

where Ileak is the leakage current that flows in a transistor when it is in off state. This power dominates dynamic power especially in deep submicron circuits and also in circuits that remains in idle mode for a long time such as cell phones. Therefore in this paper the focus is on the reduction of leakage power dissipation. The leakage current consists of various components, such as sub-threshold leakage, gate leakage, reverse-biased junction leakage, gate-induced drain leakage [3]. Among these, sub-threshold leakage and gate leakage are dominant. The sub-threshold leakage current of a MOS device can be modeled as follows [2]:

$$Isubth = I0 \exp[(Vgs-Vt) / (n\,VT)] [1- \exp(-Vds/VT)] \quad (2)$$

$$And \quad I0=\mu eff\, Cox\, (W/L)V_T^2 \quad (3)$$

Where μeff is the electron/hole mobility, Cox is the gate capacitance per unit area, W and L are width and length of the channel respectively, Vt is the threshold voltage, n is the sub-threshold swing co-efficient, VT is the thermal voltage, Vgs is the transistor gate to source voltage and Vds is the drain to source voltage. Leakage power is given by [2] previously, most of the techniques, such as MTCMOS, are focused on the leakage reduction of combinational logics, where as in this paper, we try to reduce the leakage power in sequential logics, such as flip-flops. Earlier works on flip-flops focused on characterizing them in terms of energy and energy-delay products during various transitions and presented some power-performance trade-off. Here, the focus is mainly on the characterizing the dynamic power consumption when the output changes and when the output remains the same but the clock or data change. Also, our work performs a detailed characterization of leakage power that is becoming very important in sub-250 nm regimes. Due to the tighter timing constraints and critical performances of digital systems, new flip-flop families have been developed and integrated in high performance microprocessor. Among them, DPSCRFF shown in fig.2 is assume to be the fastest. Double pulse latch flip-flop consist of pulse generator and latch part .The pulse generator generates the short duration pulse at the active clock edge and these pulses operate the latch part.

- *Sanjay Singh is currently pursuing masters degree program in ED& T in NIELIT Gorakhpur, India, PH-09450890613. E-mail: dcsanjaypm@gmail.com*
- *S.K. Singh is currently HOD department of ED & T in NIELIT Gorakhpur, India, PH-05512273874. E-mail: sks15965@yahoo.co.in*
- *Mahesh Kumar Singh is currently Assistant Professor department of ECE in BIT GIDA Gorakhpur, India, PH- 09450529806, E-mail; maheshvns@rediffmail.com*
- Raj Kumar Sagar *is currently pursuing masters degree program in ED& T in NIELIT Gorakhpur, India, PH-09956129268. E-mail: rajkrsagar@live.com*

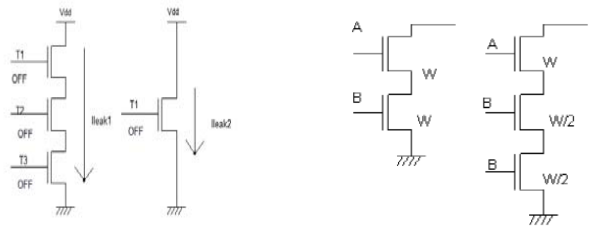
2 PROPOSED LEAKAGE CURRENT REDUCTION TECHNIQUES

In this section leakage reduction technique namely transistor stacking circuits are described.

2.1 Leakage current control using transistor stack

The leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned OFF. This effect is known as the "Stacking Effect". When two or more transistors that are switched OFF are stacked on top of each other (refer fig.1.a) then they dissipate less leakage power than a single transistor that is turned OFF(fig.1.b). This is because each transistor in the stack induces a slight reverse bias between the gate and source of the transistor right below it, and this increases the threshold voltage of the bottom transistor making it more resistant to leakage. Therefore in fig. 1(a) transistor T2 leaks less current than transistor T1 and T3 leaks less than T2. Hence the total leakage current through the transistors T, T2 andT3 is decreased as it flows from Vdd to Gnd. So Ileak1 is less than Ileak2. If natural stacking of transistors do not exist in a circuit, then to utilize the stacking effect a single transistor of width W is replaced by two transistors each of width W/2

[refer figure 1 (c)].



(a) (b) (c)

Fig.1 Transistor Stack Effect

3 PULSE TRIGGRED FLIP-FLOP DESIGN

Pulse-triggered flip-flops generate pulses during the active edge of the clock, which in turn would result in a transition at the output. This technique makes the flip-flop switch faster, but with the cost of having more power dissipation due to the glitches in the output and the internal signals. This is the case especially with the hybrid latch flip-flop (HLFF), which has very low propagation delay, setup and hold time. The setup time is found to be 0 and the hold time is 0.2 ns with the worst-case propagation delay of .09 ns. As expected the transition power consumption is very high. The clock power here is sometimes greater than the transition power, especially when the data line is one. This may be due to the spurious transitions at the internal nodes caused by the clock. A relatively low leakage power may be attributed to the large number of stacked transistors in this design. But the state dependency of leakage power is found to be high with the percentage difference being 97%.

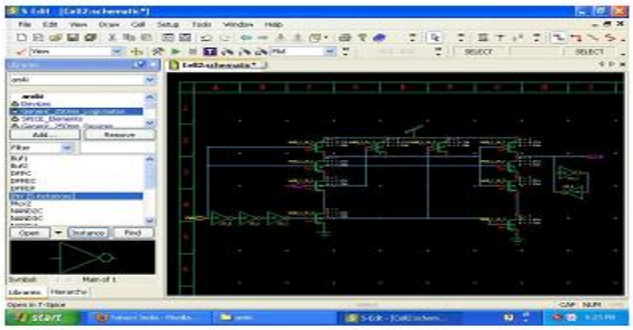


Figure 1.1 HLFF

Power Characterization of HLFF:

Output States =>	Q = 1	Q = 1
States	Avg. Power (µW)	Leakage power(µW)
D 0 ,C = 1	8.891	7.46
D 1 , C = 1	7.43	4.499

The sense-amplifier based flip-flops (SAFF) used in the StrongArm100 are evaluated here. The advantage of using such flip-flops is that they are highly sensitive to input transition. The SR latch made of NAND gates at the output stage is the major bottleneck in terms of both power and performance. This design has a propagation delay of 0.593ns. It's setup and hold times are similar to that of the HLFF. Further, this design consumes the least transition and leakage power when compared to the other designs considered here.

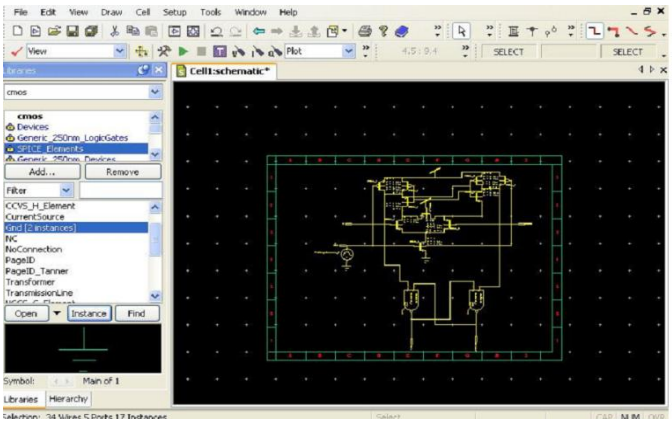


Figure 1.2 SAFF

Power Characterization of SAFF:

Output States =>	Q = 1	Q = 1
States	Avg. Power (µW)	Leakage power(µW)
D 0 , C = 1	6.855	5.845
D 1 ,C = 1	5.889	4.856

3.1 Double pulse set conditional reset flip- flop

The DPSCRFF is composed of two pieces the first one is a static set reset latch and second is pulse generator. The DPSCRFF is a single ended static flip-flop design with a single logic stage which can include arbitrary logic functionality.

Working of DPSCRFF

The working of DPSCRFF depends on two stages**:**

i. Double pulse generator:

The two pulses are generated by a local pulse generator. The width of the pulses is controlled by the inverter delay chain and this inverter in the chain can be skewed to control the lengths of p1 and p2.the width of p2 determines the transparency window of latch. For designing any flip-flop setup and hold time should not be more. In DPSCRFF to reduce setup and hold time requirements p2 should be made as small as possible.

ii. Operation of static latch:

The latch requires two clock pulses p1 and p2, which are generated from active clock edge. The first pulse preset the output node high using the p-type pull-up. The second pulse conditionally resets the output node, based on the value of the data input. The precharge causes the glitches at the output node whenever the output is supposed to remain low. An

additional inverter can be added to the output stage to isolate the storage node from the output load.

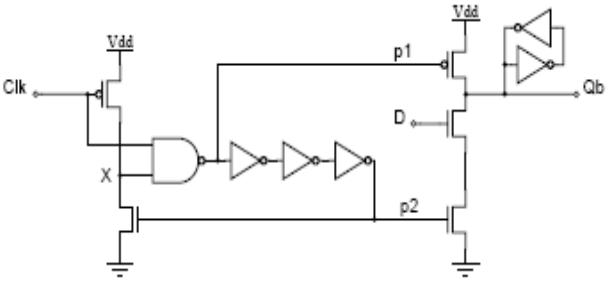


Figure 2 DPSCRFF

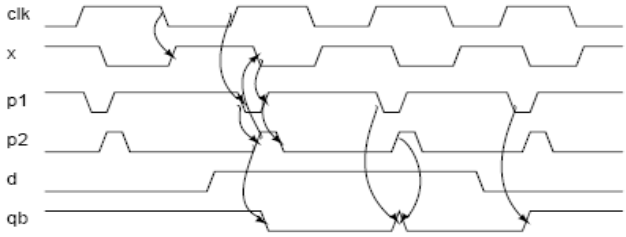


Figure 2.1 Operation of DPSCRFF

3.2 Analysis

From the BSIM MOS transistor model, the Sub threshold-leakage current can be given by:

$$I_{DS} = I_0 e^{\left(\frac{V_{GS}-V_{th0}+\gamma V_{BS}+\eta V_{DS}}{\eta V_T}\right)}(1-e^{-V_{DS}/V_T})$$

Where VT = KT/q is the thermal voltage, VGS, VDS, and VBS are the gate-to-source, the drain-to-source, and the bulk to source voltages, respectively. γ and η are the body effect and DIBL coefficients and

$$I_0 = \mu_0 C_{ox} W_{eff}/L_{eff} V_T^2 e^{1.8}$$

From fig.2., we can find although a transistor is off, there still exist a current flowing through this transistor which results in the leakage power. Fig.3 shows the keeper in DPSCRFF. When node (a) is assume to perform low to high transition, node (b) will perform high to low transition after the delay time of an inverter. Hence, before node b is stabilized as the low voltage 0, N0 transistor is still turn on. As a result when node (a) is charged, a leakage path will exist and cause extra power consumption. Similar analysis can be done when node (a) is assumed to perform high to low transition.

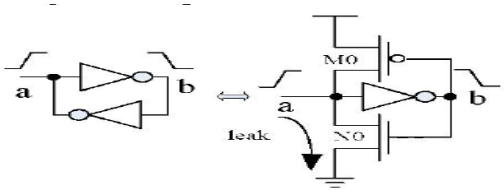


Figure 3.Keeper Analysis in DPSCRFF

4 PROBLEMS IN CONVENTIONAL DPSCRFF

There are some disadvantages in the DPSCRFF which make It slow and take large power during operation. Some problem is given below:

- This design has large number of intermediate node and thus dissipate significant amount of power.
- In this design, p1 and p2 overlap by some amount hence extra power caused by DPSCRFF.
- Large number of inverter in the pulse generator circuit for generation of pulse so large delay occurs.
- The output of the DPSCRFF has a glitch in the case where Q_b is to stay low so this glitch cause additional power dissipation in the downstream logic.
- If the clock is running and data is held high, the DPSCRFF actually dissipates more power than for the full activity waveform because of its output glitches.

Improvement

We propose a new circuit to reduce the leakage power, as shown in fig.4.The output keeper is simplified and improved for leakage reduction. When Q is assumed to perform high to low transition, PMOS 5 become turned on while NMOS 4 turned off i.e. leakage path is blocked and due to this the leakage power is reduced.

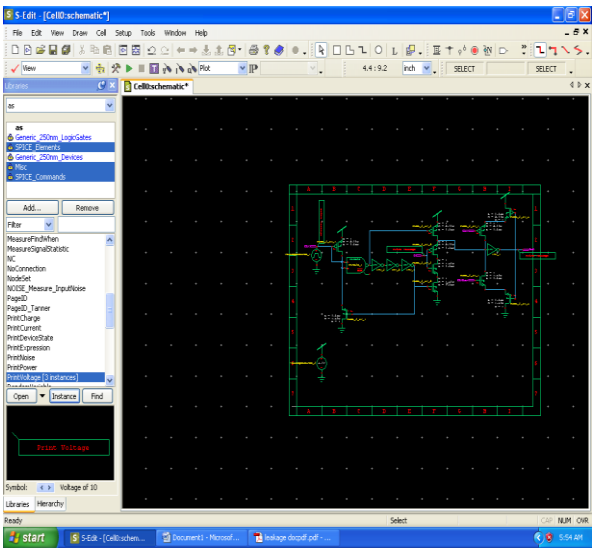


Fig4. Proposed new double pulse flip-flop

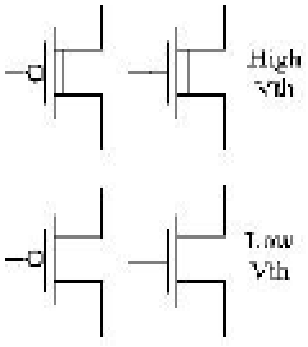


Figure 5 Symbol definition

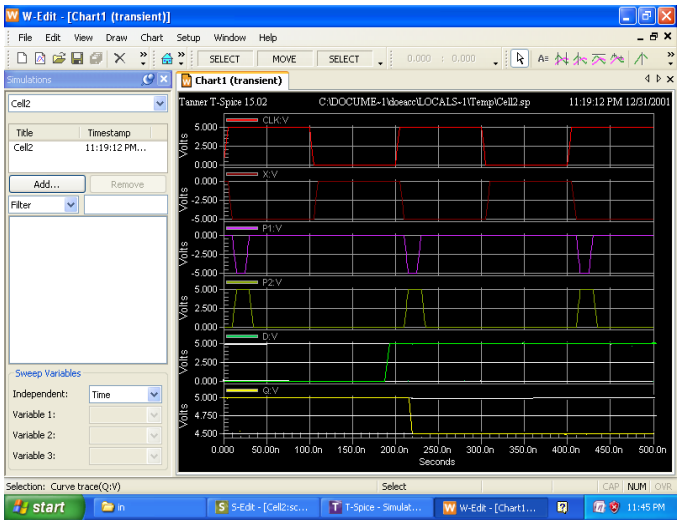


Fig 6 wave form of DPFF

Evaluation and Simulation result

I have simulated the circuit in Tanner software TSPICE. It shows comparison of leakage power in DPSCRFF and other Flip-flops.

Leakage power comparison

In the schematic of proposed new Double pulse flip-flop different threshold voltages are used both for NMOS and PMOS transistor. High speed NMOS (PMOS) transistor feature Vth=0.35v(0.45).Low leakage NMOS(PMOS) transistor feature Vth=0.54v(0.65). The minimum length and width for high speed NMOS/PMOS transistors are L=0.25u, W=0.45u.The minimum length and width for low speed NMOS /PMOS are L=0.25u, W=0.37.

The power can be calculated by using formula:

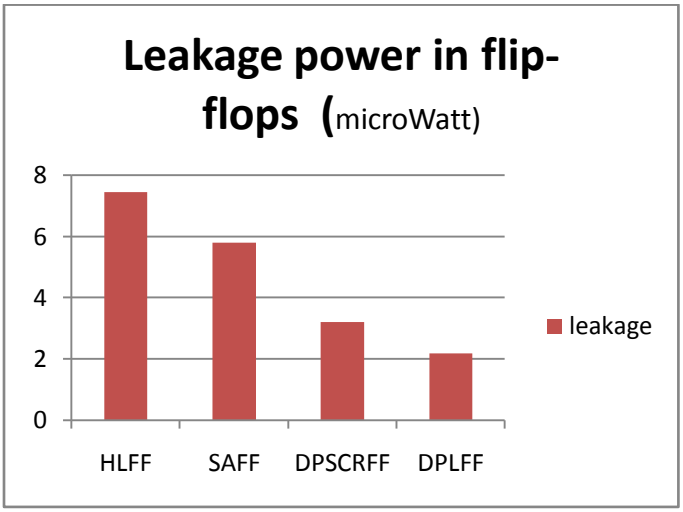
$$P(t1,t2) = \frac{1}{t1}\int_{t1}^{t2} P(\tau)d\tau$$

Average power consumption DPSCRFF and DPFF:

From the result it shows that DPLFF consumption is less compare to DPSCRFF.

Table of Comparison of double pulse flip-flops:

Average power consumed in double pulse flip-flops	DPSCRFF	DPSCRFF (Leakage power)	DPLFF	DPLFF (Leakage power)
1.	3.61µw	3.21µw	2.8µw	2.2µw



5 CONCLUSION

In this paper, we first analyze the leakage power consumption in the Pulse triggred flip-flop. A detailed comparison was also presented. We believe this characterization will be useful for other works in determining the choices of power-efficient flip-flops. Then we propose a new double pulse flip-flop, to reduce leakage power using Transistor staking technique. Experimental result shows that the proposed double pulse flip-flop behaves better than the original one even when the supply voltage is change.

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