# Performance Analysis of Dg Mosfets With High-K Stack On Top & Bottom Gate

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Abstract— In this paper we analyze the performance and characteristics of DG MOSFET with high-k material on both top and bottom gate stack and compare those with conventional pure SiO2 DG MOSFETs. We investigate the performance of the device in terms of drain current, threshold voltage and subthreshold slope using 2D quantum simulator nanoMOS 4.0. The noticeable impact of temperature is also observed both on the threshold voltage and subthreshold characteristics. This structure shows improved performance, achieved by scaling the gate length and illustrates its superiority over conventional DG MOSFETs and DG MOSFETs with only top gate stack in achieving long term ITRS goals.

Index Terms— Double Gate MOSFETs, Ballistic Drain Current, High-k Gate Stack, ITRS, Quantum Ballistic Transport Model, Subthreshold Slope, Threshold Voltage.

## 1 INTRODUCTION

The scaling of MOSFETs as dictated by the International Technology Road Map for Semiconductors (ITRS) has continued unabated for many years and enabled the worldwide semiconductor market to grow at a phenomenal rate. As device dimensions are continued to be scaling down for high performance and low power operation, thinner gate oxides are required now for nanoscale devices. However, the ITRS scaling is reaching hard limitations. One of the most significant problems is the maintenance of electrostatic integrity, which demands the use of extremely thin gate oxides, below 1 nm, to provide the required high gate capacitance, as well as the use of high channel doping to control short channel effects. These requirements lead to low device performance and tunneling current becomes quite prominent. One promising solutions to these problems is the introduction of The Double Gate (DG) MOSFET that performs more efficiently compared to its single gate (SG) bulk counterpart. DG MOSFETs have better control over short channel effects (SCE), threshold voltage roll-off, drain induced barrier lowering (DIBL) and provides reduced subthresholdslope than SG MOSFETs [1]. According to ITRS logic requirements of 2011, the required thickness of the SiO2 layer for high performance (HP) operation is to be 0.72 nm beyond 2016 and 0.54 nm after 2020 [2]. Hence, new materials are needed to satisfy both the scaling requirement and reduction of tunneling current.


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Double Gate MOSFETs with high-k gate stack is an effective solution of this problem [4, 5]. Many high-k materials have been investigated as an alternative gate dielectric based on their interface quality, band alignment to silicon and reliability [3]. In [17] different promising high-k material has also been studied based on their dielectric constant, barrier height, electron effective mass etc. DG MOSFETs with high high-k material structure allows the use of physically thicker oxide and as a consequence a reduction in gate leakage current, while still maintaining the necessary large gate capacitance. In order to improve the requirement for high doping this device architecture is able to provide increased electrostatic integrity without the need for high channel doping. These advantages makes the high-k gate stack structure eligible compared to pure SiO2 DG MOSFETs to meet future ITRS requirements [2]. Performance of bulk MOSFETs with high-κ gate stack has been studied in [6]. A comparative study of gate leakage current for DG high-κ stack gate MOSFETs using 2D and 1D Schrodinger-Poisson solver has been performed in [7]. In [4], DG MOSFET with top gate high-κ gate stack design is discussed where maximum on-current is achieved for a specified offcurrent for EOT of 0.5nm. However it is expected that performance improvement at an EOT beyond 0.5nm might be difficult due to presence of inversion layer capacitance underneath the gate dielectric as well as interfacial capacitance between the gate dielectric and metal electrode, both connected in series [8]. Therefore, there is a question if we could obtain anymore increase in the drain current while keeping the top gate EOT 0.5 nm. In this work, performance and characteristics of DG MOSFETS with both top and bottom gate stack is studied and compared with both conventional DG MOSFETs and DG MOSFETs with only top gate stack. The Quantum transport model has been widely used in literature in recent years to investigate the quantum mechanical effects on device performance [1, 5, 9]. Although scattering effects are likely to be present in such devices, for channel thickness tSi ≤10 nm, inelastic scattering process involvesenergyrelaxation that helps the MOSFET to achieve ballistic current [1]. Hence, this work utilizes the ballistic transport model toinvestigate and compare the performance of DG MOSFETs with high-kstack on both gate in terms of threshold voltage (Vth), subthreshold characteristics,

temperature effects, drain current in both the low and high drain voltage regions and effect of gate scaling according to ITRS requirements [2]. Thus a complete analysis about the performance of this device structure operating in the ballistic limit in the channel with ITRS specification will be discussed in this paper.

## 2 THEORY

In this work we used nanoMOS 4.0 to simulate planner DG structure with nonequilibrium Green's function (NEGF) approach [15]. 2D Poisson and Schrodinger's equations are solved in this model self consistently using decoupled mode space approach. The Poisson's equation is first solved with the charge from an initial band profile as the estimated potential. Then for each vertical device slice along transport direction (x) in the channel, the Schrodinger's equation is solved to obtain a set of Eigen-energies and Eigenfunctions (modes) along the gate confinement direction (z), given as [15, 16]

$$-\frac{\hbar^2}{2m_z^*}\frac{\partial^2}{\partial z^2}\Psi_i(x,z) + E_c(x,z)\Psi_i(x,z) = E_i(x)\Psi_i(x,z) \qquad (1)$$

where $m_z$* is electron effective mass in z direction, $E_c(x,z)$ is the energy of the bottom of the conduction band and $\Psi_i(x,z)$ and $E_i(x)$ are the wavefunction and Eigenenergy respectively for subband*i* at slice *x*. The 2D electron density for a subband*i* at a longitudinal energy *E* is expressed as:

$$n_i = \frac{1}{a}\sqrt{\frac{m_y^*\, kT}{2\,\pi^3\hbar^2}}\left[F_{-\frac{1}{2}}(\mu_S - E)A_s - F_{-\frac{1}{2}}(\mu_D - E)A_D\right] \qquad (2)$$

where*a* is grid spacing along the x direction; $\mu_S$, $\mu_D$are Fermi levels at source and drain respectively. $A_S$,$A_D$are corresponding spectral density functions, $F_{-1/2}$is the Fermi-Dirac Integral of order (-1/2), $m_y$* is electron effective mass in y direction, *k* is Boltzmann's constant and *T* is the operating temperature. The resulting spatial charge distribution from net 2D charge density obtained from all subbands in the quantum well is inserted in the Poisson equation to update a new potential profile. This process is continued until the desired convergence is achieved. Finally, the quantum ballistic current and transmission coefficient are calculated for each subband. Thus, the ballistic drain current $I_i$ is readily obtained by summing up the currents from all subbands expressed as:

$$I_i = \int_0^\infty I_i(E)dE \qquad (3)$$

Where,

$$I_i(E) = \frac{q}{\hbar^2}\sqrt{\frac{m_y^*\, kT}{2\,\pi^3}}T_i(E)\left[F_{-\frac{1}{2}}(\mu_S - E)A_s - F_{-\frac{1}{2}}(\mu_D - E)A_D\right]$$

Where $T_i(E)$ is the transmission coefficient from source to drain and $I_i$ *(E)* is the subband current at longitudinal energy *E* of subband*i*. This decoupled mode space is an efficient and accurate simulation method for modeling nanoscale MOSFETs and shows excellent agreement with full 2D real space discretization [16]. Hence, this model has been used in this work for characterization of the DG MOSFET with high-κ material in top and bottom gate stack in nano scale region.

## 3 DEVICE STRUCTURE AND PARAMETERS

A Schematic cross sectional view of a DG MOSFET with high-k gate stack on both top and bottom gate is shown in fig.1. The background doping of the silicon film is considered to be intrinsic and the source and drain doping is $2\times10^{20}$ $cm^{-3}$.According to [5] a thicker body reduces the series resistance and effect of process variation but also degrades the short channel effect, so thinner film is preferable from SCE point of view but it is difficult to fabricate uniformly. In this work silicon film thickness is considered to be 3nm .For DG MOSFET with both top and bottom gate stack, top $SiO_2$ interfacial layer is stacked by $La_2O_3$ which is considered to be gate dielectric for high-k gate stack. $La_2O_3$ has been used regarding its future possibility of being practical high-k dielectric material for reduced Equivalent Oxide Thickness (EOT) values which has been recently experimentally confirmed [10]. The bottom $SiO_2$ interfacial layer is also stacked with high-k dielectric whose thickness and dielectric constant is varied in the simulation process. EOT of 0.5 nm is considered for DG with only top gate stack. For conventional DG with pure $SiO_2$ gate dielectric, the top oxide thickness has been set as $t_{ox1}$= $t_{ox2}$=1.2 nm since it is the lowest thickness limit that can be achieved with pure $SiO_2$ satisfying the gate leakage requirements [4].Constant mobility is considered in source, drain, and channel region.

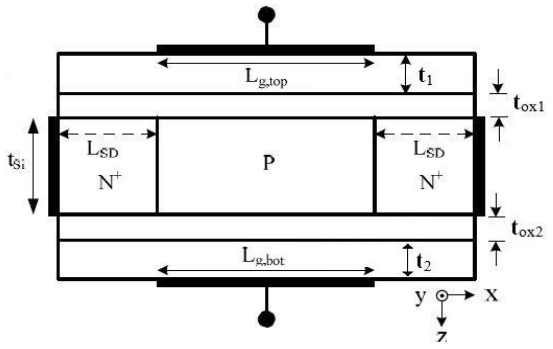



Fig. 1. Schematic Diagram of DG MOSFET with high-k stack on top and bottom gate.

## 4 RESULTS & DISCUSSION

The simulation is performed to explore the improved characteristics of DG MOSFETs with both gate stack and to compare those with DG MOSFETs withonly top gate stack and conventional DG MOSFETs.

### 4.1 Effect on Threshold Voltage and Drain Current

In DG with both gate stack, bottom gate high-k plays an important role on electrostatic control since electric field generated by the drain can be curved into the bottom oxide and take part into potential barrier lowering in the channel entrance [14]. Fig. 2(a) shows as the bottom gate high-k layer thickness is increased from 1.5 nm to 6 nm there is a significant decrement in source to drain potential barrier. This result is in clear agreement with [18]. Due to the decrement of potential barrier there is a significant increase of electron density in channel region. The increase of electron density can be seen in fig. 2(b) as the bottom gate high-k thickness is increased.

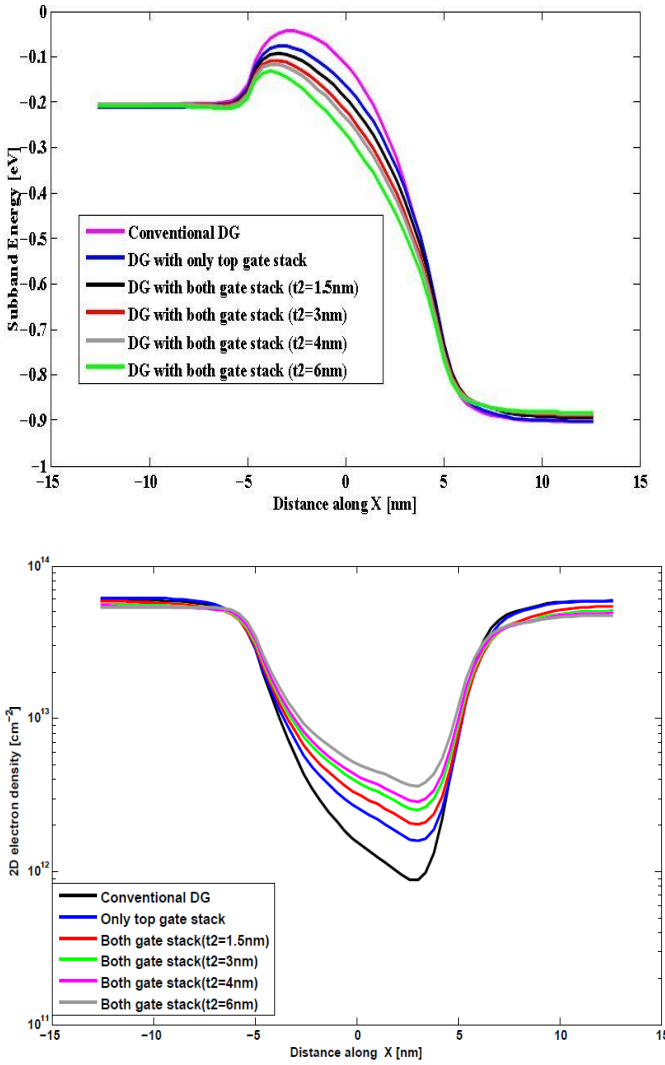



Fig. 2. (a) Variation of subband energy along the channel. (b) Electron density in a subband at strong inversion.

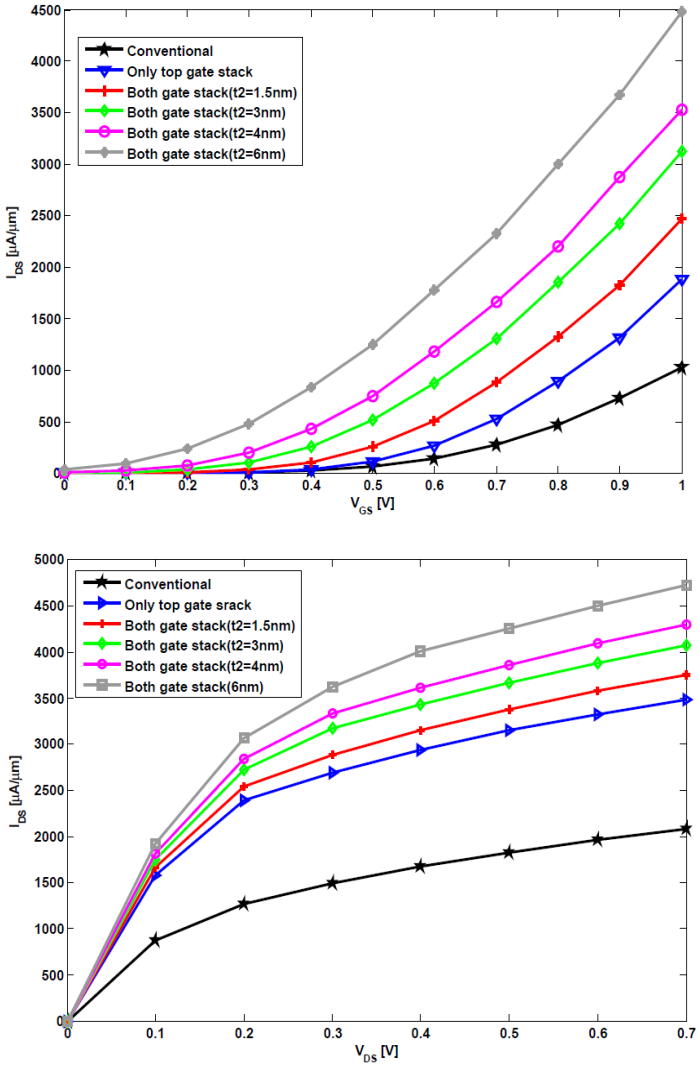



Fig. 3.(a) ID-VGS characteristics comparison showing lower Vth for DG MOSFETs with both gate stack. (b) ID-VDS characteristic comparison showing higher drain current with thickness variation at both low and high drain voltage operation.

This increased electron density results in a reduced threshold voltage.Fig. 3(a) clearly shows the reduction of threshold voltage according to the incremental thickness of bottom gate high-k material which is much less than conventional DG and DG with only top gate stack of EOT 0.5. Drain current is also improved as the bottom gate high-k layer thickness is increased from 1.5nm to 6nm. Fig. 3(b) shows the improvement in drain current for DG with both gate stack which is about 25.4% more compared to DG with only top gate stack. An improvement on threshold voltage and drain current could also be obtained by keeping the device dimensions constant and varying the dielectric constant of bottom gate high-k material. Fig. 4(a) shows a decrement in potential barrier when dielectric constant of bottom gate stack is decreased from 30 to 10 which is in agreement with [18]. It results in a improvement in electron density shown by Fig. 4(b) and reduction of threshold voltage in Fig. 5(a) for DG MOSFETs with both gate stack.

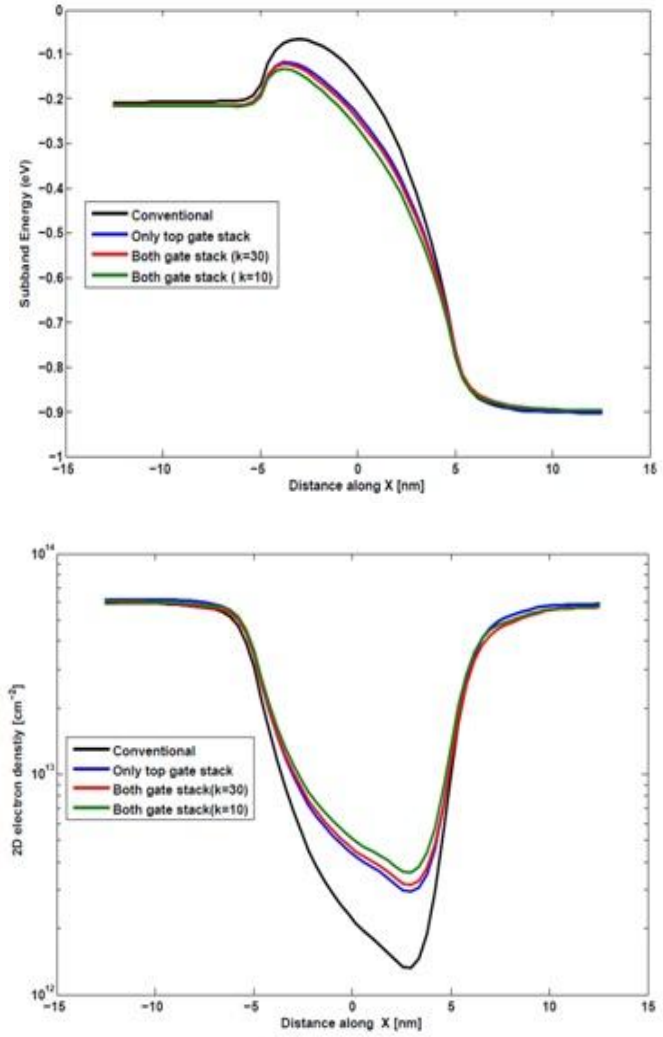
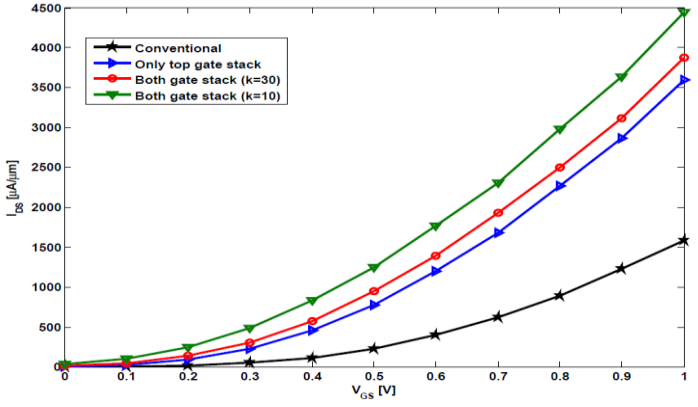



Fig. 4. (a) Variation of subband energy along the channel. (b) Electron density in a subband at strong inversion.

The improvement in drain current is shown in Fig. 5(b). About 15% improvement in drain current is achieved for DG with both gate stack compared to DG with only top gate stack.Future generation devices will be driven at lower threshold voltage and high drain current. In this paper, we've shown that this device gives better performance for threshold voltage and drain current than conventional DG and DG with only top gate stack.



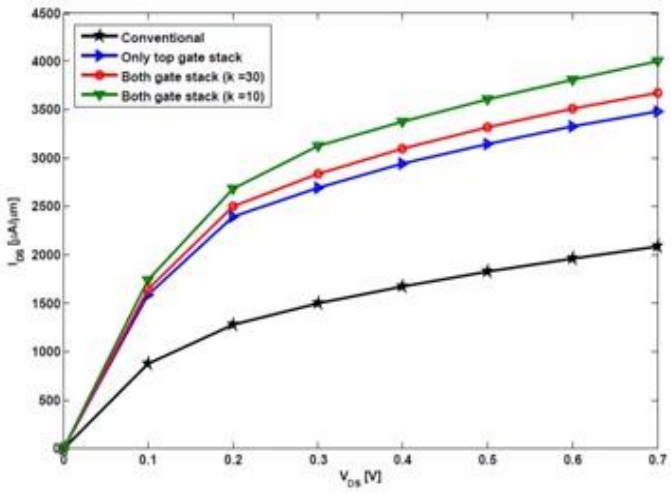
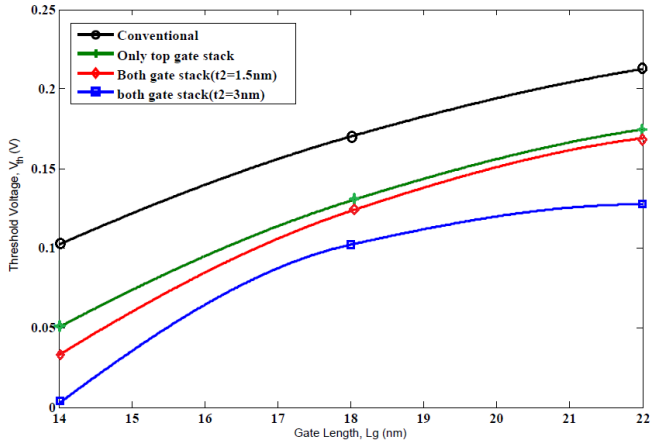




Fig. 5.(a) ID-VGS characteristics comparison showing lower Vthfor DG MOSFETs with both gate stack. (b) ID-VDS characteristic comparison showing higher drain current with dielectric constant variation at both low and high drain voltage operation.

## 4.2 Effect of gate length on device performance

Apart from introduction of bottom gate stack, another way of improving the device performance is by increasing the amount of inversion charges underneath the gate by scaling down the device geometry. According to ITRS 2011 high performance (HP) logic technology requirements, DG MOSFET physical gate length at year 2012 will be 22nm whereas beyond 2014, the gate length will scale down at 18 nm followed by 14 nm after 2017 and 10.6 nm after 2020[2]. Hence, in accordance to the ITRS specification, performance of DG MOSFETs with both gate stackshould be evaluated. According to ITRS 2011 updates, supply voltage (Vdd) will stay around 0.8V at 2012 and decrease near 0.7V at 2019[2]. In this section device performance is observed with gate length variation while keeping all other parameters same. This simulation was performed at supply voltage of 0.7V. For high-k gate stack at both gate, simulation result suggests that as gate length is scaled down to10.6 nm from 22 nm drain current is improved by 39.15%, shown in Fig. 6. (a)



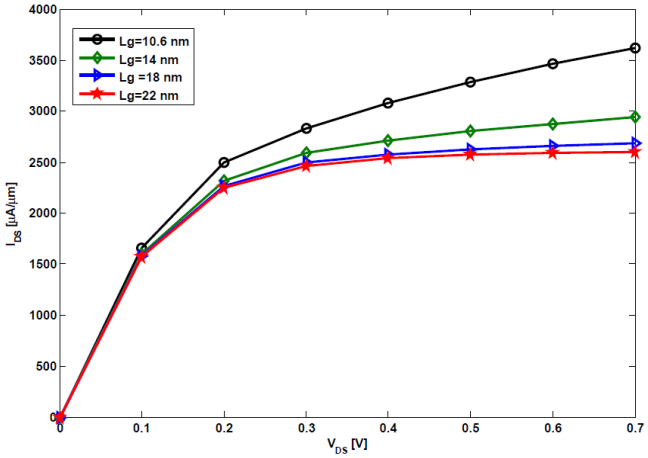


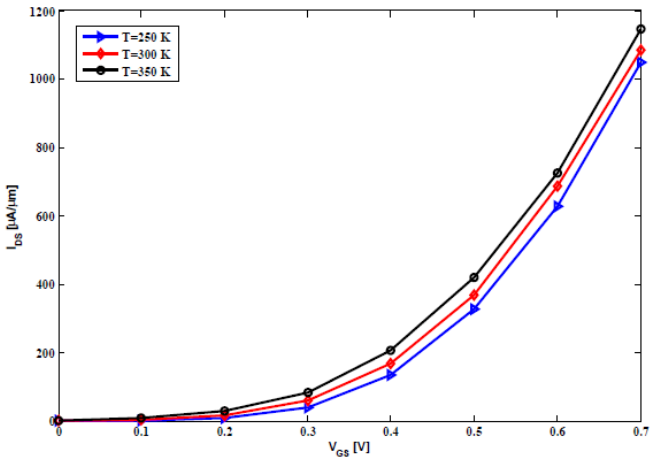

Fig. 6.(a) Performance improvement of of DG MOSFET with both gate stack with gate scaling according to ITRS specification of 2011[2]. (b) Reduction threshold voltage with gate length.

Decrement in threshold voltage is another benefit that is achieved as the gate length is scaled down. Fig. 6(b) shows the reduction of Vthwith gate scaling for DG MOSFETs with both gate stack, DG MOSFETs withonly top gate stack and conventional DG case.

## 4.3 Temperature dependence of threshold voltage

Threshold voltage is sensitive and varies with operating temperature. Quantum ballistic transport model suggests that 2D electron density of each subband increases with temperature as indicated by (2). As a result there is an increment of subband current for that longitudinal energy. This increment isfollowed by the increase in drain current and simultaneous reduction of threshold voltage. Fig. 7 shows the reduction of Vthand corresponding increase in drain current for high-k material on both gate stack(t2=3 nm) with increasing temperature.

Fig. 7. Effect of temperature on threshold voltage of a DG MOSFET with both gate stack having with t2=3 nm.



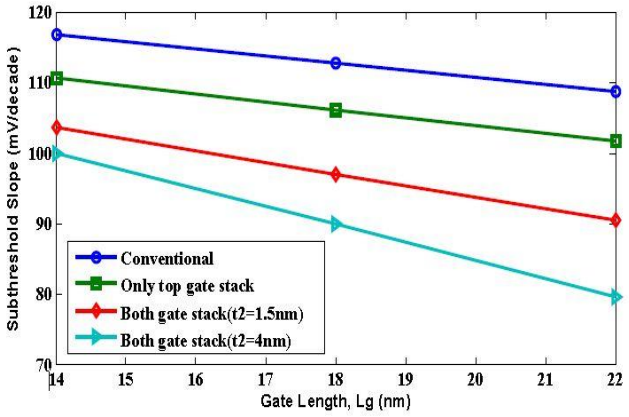

## 4.4 Analysis of subthreshold characteristics

Low voltage and low power application requires a lower value of subthreshold slope for better gate controllability. Various factors affect the subthreshold slope of the device such as: gate oxide thickness, temperature, interface trap density, doping concentration etc [11]. The subthreshold slope for double gate MOSFETs is expressed as [12]:

$$S = 2.3\,\frac{kT}{q}\left(1 + \frac{C_{it1}}{C_{ox1}} + \frac{C_{ox2} + C_{it2}}{C_{ox2} + C_{it2} + C_{Si}}\frac{C_{Si}}{C_{ox1}}\right) \qquad (4)$$

$$\simeq 2.3\,\frac{kT}{q}\,(1 + \frac{t_{ox1}}{t_{ox2}})$$

Where $C_{ox1}$and $C_{ox2}$are top and bottom gate oxide capacitances respectively, $C_{it1}$and $C_{it2}$are interface trap capacitances and $C_{Si}$is the film capacitance. Subthreshold slope has been determined by evaluating the gate voltage required to reduce the ballistic drain current by one decade in weak inversion region. According to [12] subthreshold slope gets more affected by oxide capacitance then compared to film and interface capacitance. In this work bottom oxide thickness is same for conventional DG and DG with only top gate stack while for DG with both gate stack, bottom gate high-k thickness is varied. The effect of gate length and temperature on subthreshold slope has been observed with the NEGF ballistic approach. Fig. 8(a) shows that as the gate length is scaled down from 22 nm to 14 nm according to ITRS [2] subthreshold slope decreases significantly which is supported by [13]. From (4) it is clearly observed that as the bottom gate high-k thickness is increased the total oxide thickness also increases which in terms decreases subthreshold slope that is seen in Fig. 8(a).



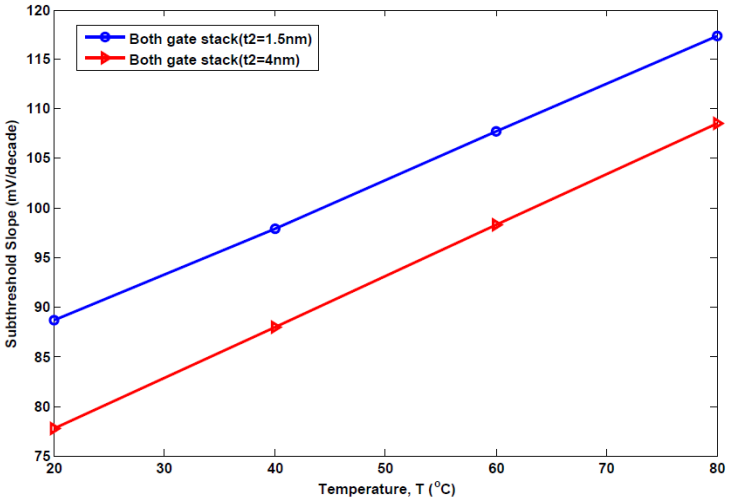



Fig. 8.(a) Variation of subthreshold slope with gate length. (b) Effect of bottom gate oxide thickness and operating temperature on subthreshold slope.

Thus, bottom gate stack oxide acts as a controlling gate oxide. Moreover, due to the improved gate controllability, DG with both gate stack is more suitable for nanoelectronic digital applications than conventional DG and DG with only top gate stack. From (6) it can also be seen that subthreshold slope increase proportionally with temperature. Variation of subthreshold slope with temperature for DG MOSFET with both gate stack is plotted in Fig. 8(b)

## 5 CONCLUSIONS

The performance of DG MOSFETs with high-kstack on both gates has been studied in this work in the context of current ITRS specifications using Quantum ballistic transport model. It has been observed that this structure will give higher drain current in the low and high drain voltage regions, as well as lower threshold voltage and improved subthreshold swing compared to high-k stack on only top gate and conventional pure SiO2 gate devices. Relative increase in the drain current and reduced threshold voltage have beenobserved for increasing subband electron density. Moreover, it is seen that the threshold voltage of the device decreases with increasing operating temperature. This has been explained with the increase of subband carrier concentration and corresponding subband current. Most importantly, it has been found DG MOSFETs with high-k stack on both gates are more compatible to meet ITRS goals of high performance devices compared to high-k stack on only top gate and conventional pure SiO2 ones and show improved performance with downscaling gate dimensions. Thus it can be predictedthat to continue scaling, DG MOSFETs with both gate stack will provide useful performance gains forfuture device requirements.

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## REFERENCES

[1] M. K. Ashraf, A. I. Khan and A. Haque, “Wave function penetration effects on ballistic drain current in double gate MOSFETs fabricated on <100> and <110> silicon surfaces,” in Solid- State Electronics., vol. 53, no. 3, pp. 271–275, 2009.

[2] The International Technoloy Roadmap for semiconductors. Available: http://www.itrs.net/Links/2011ITRS/Home2011.htm

[3] G. D. Wilk, R. M. Wallace, and J. M. Anthony, “High-κ gate dielectrics: Current status and materials properties considerations” in Journal of Applied Physics., vol. 89, 2001.

[4] M. S. Lundstrom, K. D. Cantley, H. S. Pal, “Nanoscale transistors: Physics and materials,” in Materials Research Society Symposim Proc., vol. 958, 2007.

[5] S. Hasan, J. Wang and M. Lundstrom, “Device design and manufacturing issues for 10 nmscale MOSFETs: a computational study,” in Solid-State Electronics, vol. 48, pp. 867–875, 2004.

[6] J. R. Watling, A. R. Brown, G. Ferrari, J. R. Barker, G. Bersuker, P. Zeitzoff and A. Asenov,“Impact of High-κ Gate Stacks on Transport and Variability in Nano-CMOS Devices,” in J. Computational and Theoretical Nanoscience, vol. 5, pp. 1072– 1088, 2008.

[7] Schenk and M. M. Luisier, “2D Simulation of Gate Currents in MOSFETs:Comparison between S-Device and the Quantum Mechanical Simulator GreenSolver,” in Int.Conference on Simulation of Semiconductor Processes and Devices, pp. 301–304, Sept, 2008.

[8] K. Natori, “Prospective characteristics of nanoscale MOSFETs” in IEEE International Conference on Solid-State and Integrated Circuit Technology, pp. 47-50, 2006

[9] Schenk and M. M. Luisier, “2D Simulation of Gate Currents in MOSFETs:Comparison between S-Device and the Quantum Mechanical Simulator GreenSolver,” in Int.Conference on Simulation of Semiconductor Processes and Devices, pp. 301–304, Sept, 2008.

[10] K. Kakushima, K. Okamoto, K. Ttachi, P. Ahmet, K. Tsutsui, N. Sugii, T. hattori, H.Iwai,“Further EOT Scaling below 0.4 nm for High-k Gated MOSFET,” in Int. Workshop on Dielectric Thin Films for Future Electron Devices, pp. 9–10, 2008.

[11] J.S. Lyu, “A New Method for Extracting Interface Trap Density of Short Channel MOSFETS from Substrate Bias Dependent Subthreshold Slopes,” in ETRI Journal, vol. 15, no. 2, pp. 11–25, Nov,1993.

[12] Ernst, T. and Cristoloveanu, S. and Ghibaudo, G. and Ouisse, T. and Horiguchi, S. and Ono, Y. and Takahashi, Y. and Murase, K., “Ultimately thin double-gate SOI MOSFETs,” in IEEE Trans.on Electron Devices, vol. 50, no. 3, pp. 830–838, March, 2003.

[13] D. Rechem, S. Latreche and C. Gontrand, “Channel length scaling and the impact of metal gate work function on the performance of double gate-metal oxide semiconductor field-effect transistors” in Pramana - Journal of Physics Vol. 72, No. 3 pp. 587-599, March, 2009.

[14] Simon Deleonibus, Electronic Device Architectures for the Nano-CMOS Era: From Ultimate CMOS Scaling To Beyond CMOS Devices, Pan Stanford Publishing, 2008.

[15] Z. Ren, R. Venugopal, S. Goasguen, S. Datta, and M. S. Lundstrom, "nanoMOS 2.5: A twodimensional simulator for quantum transport in double-gate MOSFETs," in IEEE Trans. On Electron Devices, vol. 50, no. 9, pp. 1914–1925, Sept, 2003.

[16] R. Venugopal, Z. Ren, S. Datta, M. S. Lundstrom and D. Jovanovic, "Simulating quantum transport in nanoscale MOSFETs: real versus mode space approaches," in J ApplPhys, vol. 92,no. 7, pp. 3730–3739, 2002.

[17] GhaderDarbandy, RomainRitzenthaler, Fran¸cois Lime, Ivan Gardu˜no, Magali Estrada, Antonio Cerdeira and Benjamin I ˜niguez "Analytical modeling of direct tunneling current through gate stacks for the determination of suitable high-k dielectrics for nanoscale double-gate MOSFETs" in Semiconductor Science and Technology, vol. 26, 2011.

[18] F.Djeffal, M.Meguellati, A.Benhaya "A two-dimensional analytical analysis of subthreshold behavior to study the scaling capability of nanoscale graded channel gate stack DG MOSFETs" in Physica E, vol. 41, pp. 1872-1877, 2009