A Novel Single Phase Five Level Inverter With Coupled Inductors And Closed Loop System

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Abstract: Multilevel inverters are very essential in the modern days because of many uses and also due to the advantage of producing many levels of voltages enabling a variety of applications such as power conditioning,active filters and motor drives.The proposed multilevel inverter enable us to produce five levels without any phase shift.The proposed technique uses pwm technique along with a feedback signal so whole circuit is implemented in closed loop.The simulation is done using matlab.The results are included to show the performance of five level inverter implemented in closed loop system

I. INTRODUCTION

The multilevel inverters are becoming popular from the time when it was proposed.Multilevel inverter means the inverter in which more than two levels are used.The multilevel inverter have many advantages such as:-1) Simple construction and easy implementation. 2)Less switching losses is compared with existing system.3)The effective control of the switches is achieved.4) This inverter can produce output five level voltages with only one dc source, by which we can avoid the voltage balancing problem in conventional multilevel inverters.5)The level of the output voltage is only half of the dc-link voltage in all conditions, leading to much reduced dv/dt.6)This inverter is based on widely used three-arm power module and the voltage stresses on all power switches are same, making it very easy to construct. Applications of this multilevel inverter includes active filters,power conditioning and motor drives.In these recent years it has been noted that the use of multilevel inverters are increasing.In the earlier days there required the use of more number of switches.In this technique it enable us to produce the output with reduced number of switches.Also we can notice that there is less dv/dt in the output side.Thus this technique is of great advantage. The disadvantages of the existing technique are:

[1]The inverter design is difficult to construct and robust in operation.

[2]The supply sources used in each bridge is doubled for each bridge.

These disadvantages are overcomed by using feedback technique. The applications include power conditioning which is athe process of improving quality of power delivered to electrical equipment.Thus it provide extra protection in power disturbances.For eg:-PC,VCR,oven,stereos It is used as a surge protection device by reducing magnitude of voltage spikes to safe level. It is also used as noise filters by blocking characteristic noise pattern and allow only desired frequency to equipment. Another application is motor drives. The advantages of this are

[1]Smooth operation

[2]Acceleration control

[3]Different operating speed

The motor drives electrical energy from the circuit and supplies it to the motor.Inverter uses modulation techniques to create needed three phase ac voltage output for motor. The frequency can be adjusted to match the need of process. The higher the frequency of output voltage is higher speed of motor. The third application is active filter.It uses amplifier. It improves the power quality.The inverter output voltage generate output current that follows respective reference current which contain harmonic and reactive component required by the load. Eg:radio,tv,cell phones

II. PROPOSED INVERTER TOPOLOGY

In the conventional multilevel inverter topologies, the multilevel inverter is used without the feedback switch.So the Waveform obtained will be shifted.So we won't get the correct output voltage. So we propose a new technique in which the waveform is not shifted.As we see we have six switches and these switches are turned on and off according to the switching states.

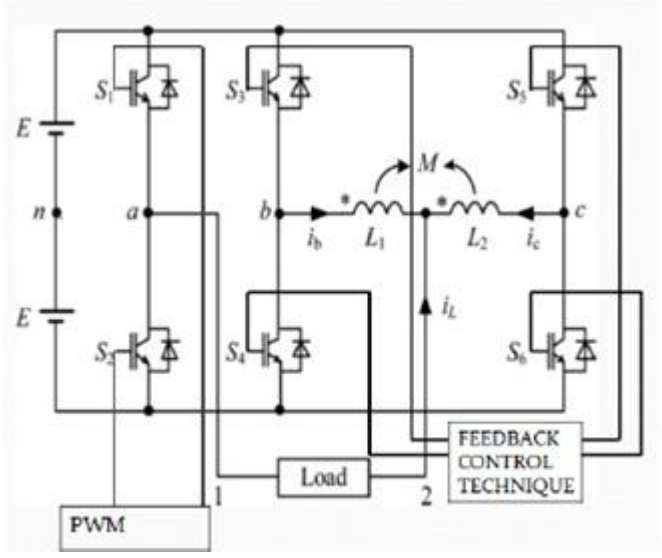

Fig. 1 Circit diagram of proposed five level inverter

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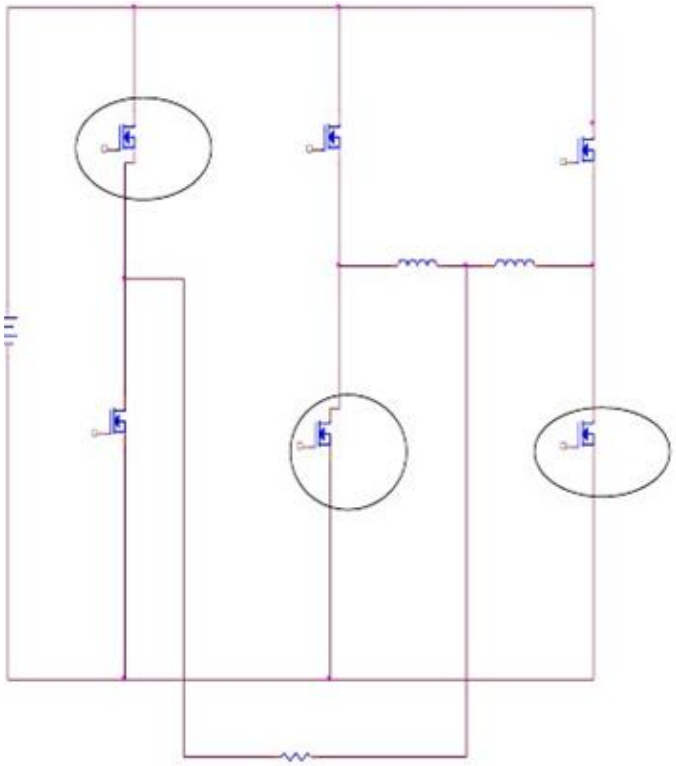
Switching states of switches:

S1	S3	S5	Vo
1	0	0	+E
1	0	1	+E/2
1	1	0	+E/2
1	1	1	0
0	0	0	0
0	0	1	-E/2
0	1	0	-E/2
0	1	1	-E

III.PRINCIPLE OF OPERATION

The principle of operation is explained through different modes:

MODE 1



OUTPUT=Vdc
Vo=(U1-U2)/2
= (E-(-E-E))/2
=2E/2
=E

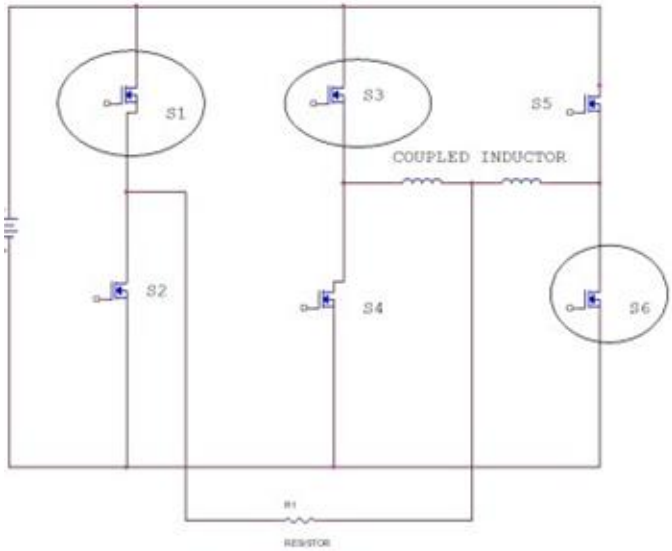
MODE 2

OUTPUT=Vdc/2

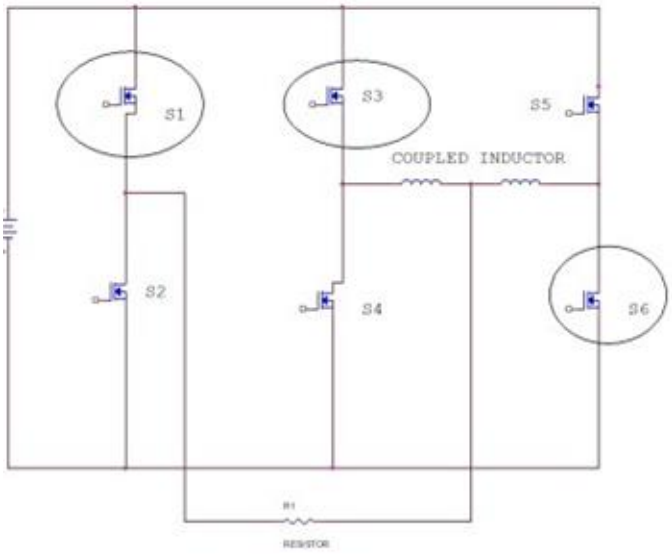
Vo=(U1-U2)/2
= (E-(-E+E))/2
=E/2

MODE 3

OUTPUT
Vo= E/2



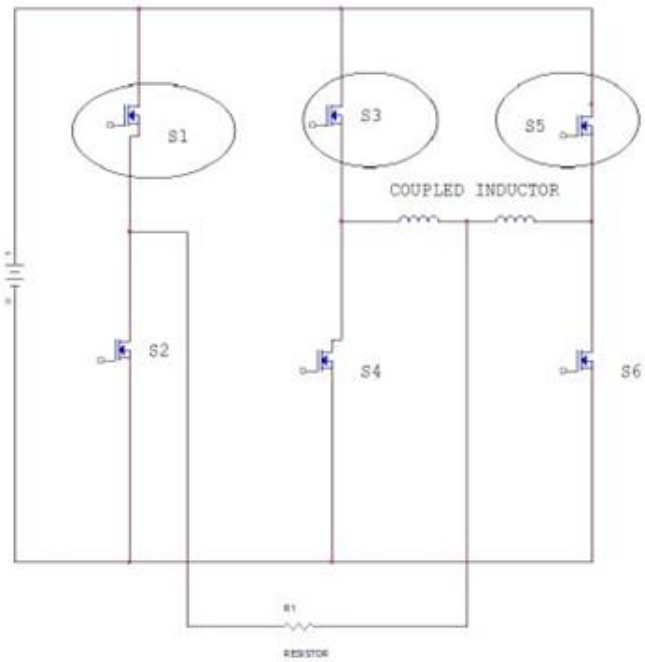
MODE 4



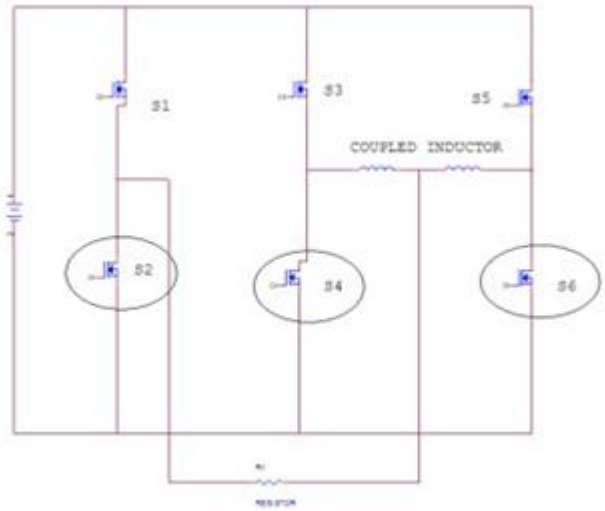
OUTPUT
OUTPUT=Vdc
Vo=(U1-U2)/2
=0

MODE 5

OUTPUT
Vo=(U1-U2)
=(Vdc-Vdc)
=0



MODE 6
OUTPUT=-E/2

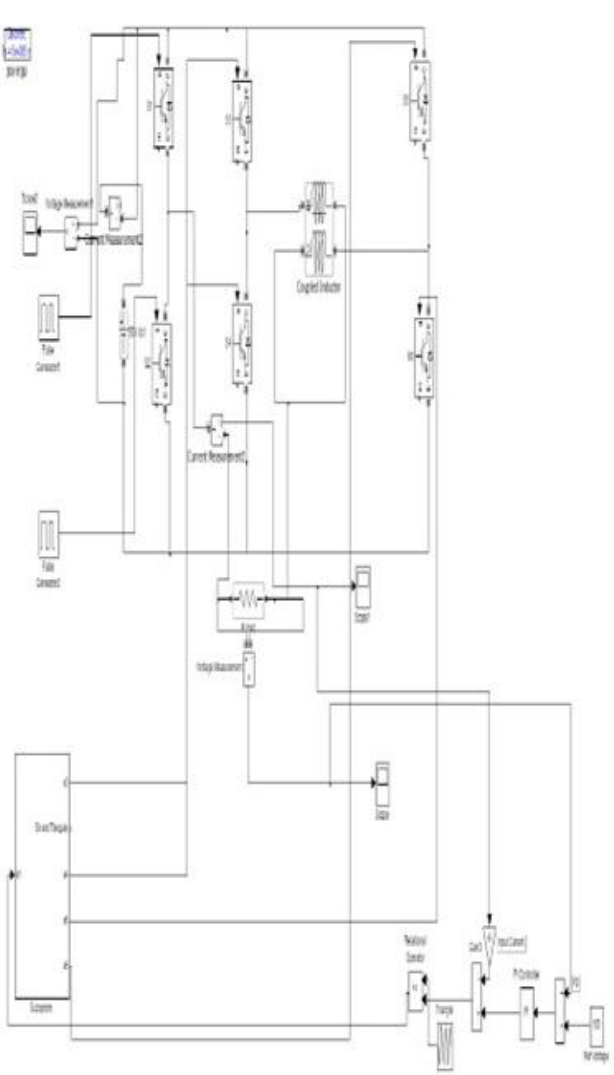


MODE 7
OUTPUT
Vo= -E/2

MODE 8

OUTPUT=-E

Matlab simulink of proposed system



The figure shows diagram of proposed topology The proposed system consists of the circuit implemented in closed loop. So an additional feedback signal is given to the circuit along with the pwm technique. So the waveform is obtained without shifting and correct output can be obtained. The obtained system is more stable as we get proper output.

CASES FOR SELECTING SWITCHING STATES OF S1,S3,S5

The switching state of S1 is decided by the sign of u12ref (the reference of u12):

S1 is 1 if u12ref ≥0 and

S1 is 0 if u12ref ≤ 0.

To decide the switching states of (S3 , S5), the following four cases will be discussed:

Case I (+E < u12ref < + 2E):
U12 between +2E and +E.
Switching states are (S3, S5).

Switching states within every Ts can be:

1.(0, 0)↔(0, 1) (defined as SS1)or

2. (0, 0)↔(1, 0) (defined as SS2).

Case II (0 ≤ u12ref < +E)
u12 is between +E and 0. Switching states are (S3 , S5).
The switching states within every Ts can be:

1.(0, 1)↔(1, 1) (defined as SS3) or

2. (1, 0)↔(1, 1) (defined as SS4).

Case III (−E < u12ref ≤ 0)
u12 is between +0 and −E. Switching states are (S3 , S5).
The switching states within every Ts can be:

1. (0,0)↔(0, 1) (defined as SS1) or

2.(0,0)↔(1, 0) (defined as SS2).

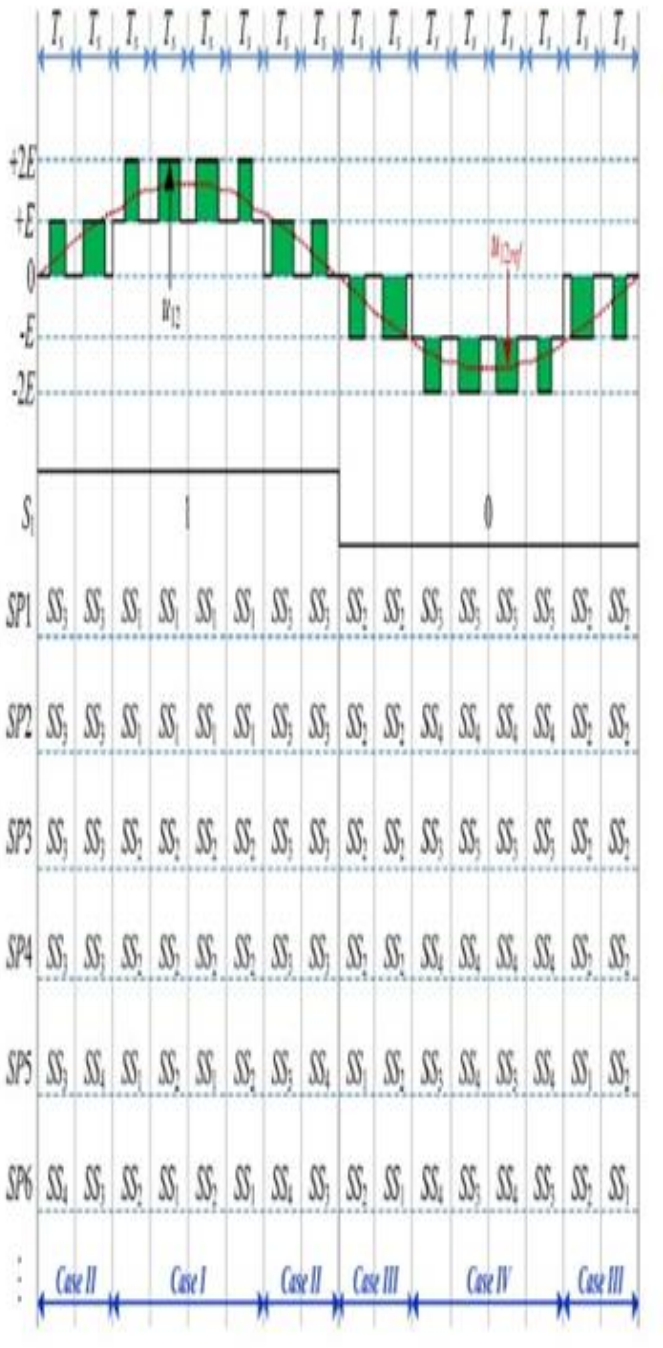
Case IV (−2E < u12ref <− E)
Voltage u12 is between−E and−2E.
Switching states are (S3,S5)
The switching states within every Ts can be :

1.(0, 1)↔(1, 1) (defined as SS3) or

2. (1, 0)↔(1, 1) (defined asSS4).

Thus the switching pattern for six switches can be obtained from these cases.

SWITCHING PATTERN FOR SWITCHES



IV.MATHEMATICAL CALCULATIONS

If the two coupled inductors are with the same number of turns or obtained by a center-tapped inductor. The leakage inductances of the two inductors are Lσ1 and Lσ2, respectively. Assuming that Lσ1 = Lσ2 = Lσ, the voltage equations of the coupled inductors can be expressed as follows:

$$(M + L\sigma)\frac{dib}{dt} - Mdic = ubn - u2 \quad \text{.....(1)}$$

$$(M + L\sigma)\frac{dic}{dt} - Mdib = ucn - u2 \quad \text{.....(2)}$$

Meanwhile, according to Kirchhoff's current law,we obtain:

ib + ic + iL = 0 ..... (3)

From (1) to (3), the following equation can be derived:

$$u2 = \frac{(ubn + ucn + L\sigma \frac{diL}{dt})}{2} \quad \text{.....(4)}$$

Generally, the leakage inductance can be designed to be very small and (4) can be rewritten as

$$u2n = \frac{(ubn + ucn)}{2} \quad \text{.....(5)}$$

Therefore output voltage u12 is

$$U12 = u1 - u2 = u1 - \frac{(ubn + ucn)}{2}$$

V. MATHEMATICAL DESIGN

INDUCTANCE VALUE

M=(Ts*E)/(IL)
=(20*10^-6*48)/(1)
=0.96*10^-3
=~1*10^-3

DESIGN FOR SWITCH S1 &S2
FREQUENCY = 50HZ
TIME PERIOD = (1)/(50)
= 20Ms

PULSE WIDTH = Ton/Ts
=(10*10^-3)/(20*10^-3)
=50Ms

DELAY FOR S1 = 0Ms
(delay is 0 as its first switch)
DELAY FOR S2 = 10Ms
(delay is Ton of S1 is S2)

WHERE
M-Mutual inductance
M= (Ts*E)/(IL)

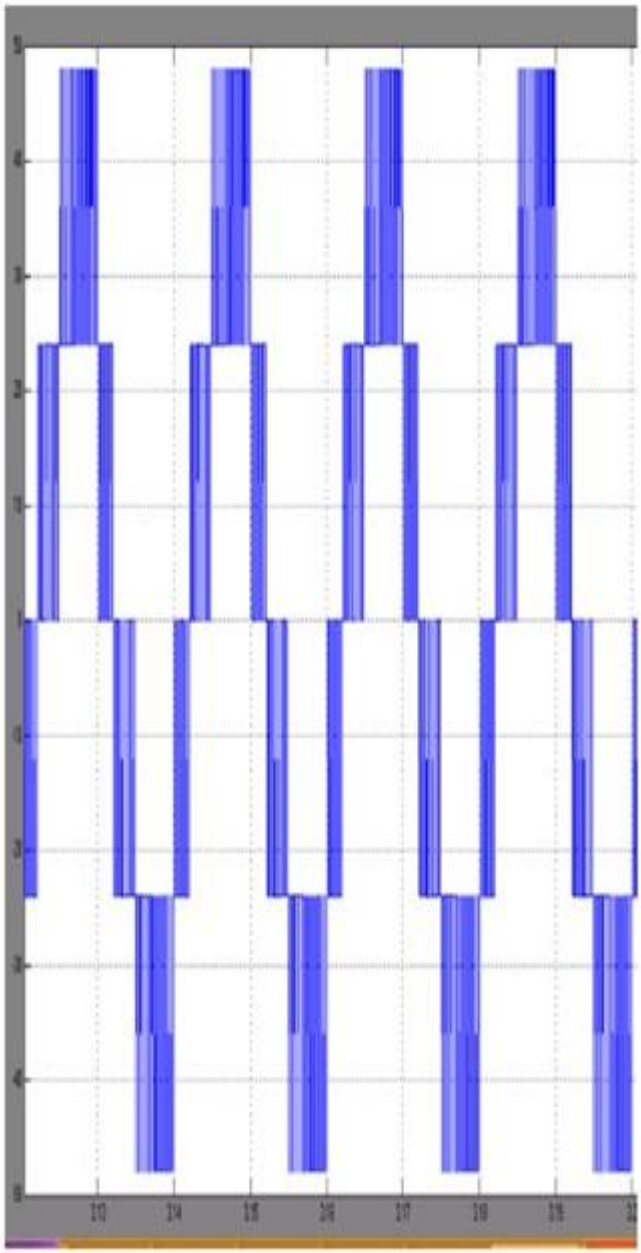
Ts-Time period
E- Output voltage
E=(U1-U2)/2

I- Current
L- Self inductance
F-Frequency
F=1/Ts

Ts-Time period
Ts=Ton+Toff

Ton-On time of switch PW-pulse width
PW=(Ton)/(Ton+Toff)

V1.SIMULATION RESULTS



The five levels of voltage are at 0,25,50,-25,-50 volts. The input voltage is 48v INVERTER PARAMETERS

Dc-link voltage	100 V
Mutual inductance	M=3 mH
Load inductance	L_L=8.3 mH
Load resistance	R_L=20 Ω
Carrier frequency(S_3- S_6)	4 kHz

VII. CONCLUSION

This paper proposed a novel single-phase five-level inverter based on coupled inductors. This inverter can output five-level voltage with only one dc source,no split of the dc voltage capacitor, totally avoiding the voltage balancing problem. The proposed technique which include pwm and feedback technique enable us to get five levels of voltage with no shift of waveforms.The voltage stresses on all the power switches are the same and only four switches are operated at high frequency. Operation mechanism of this inverter was analyzed and the optimized switching patterns were also presented to
minimize the passive component.

VIII REFERENCES

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