Design Of Area And Speed Efficient Square Root Carry Select Adder Using Fast Adders

K.Mariya Priyadarshini, N.V.N. Ravi Kiran, N. Tejasri, T.C. Venkat Anish

Abstract: Area and speed are the most important design objectives in integrated circuits. As addition is the basic operation of all computer arithmetic, adders are one of the widely used components in digital integrated circuit design. Since propagation of carry is of major concern in designing efficient adders, this paper presents different fast adders and their performance analysis. Among all the adders discussed Square root Carry Select Adder (SQCSA) provides a good compromise between cost and performance. As, Conventional SQCSA is still area consuming due to dual Ripple Carry Adder(RCA)structures, modifications are done at gate level to reduce area. Modified SQCSA is designed using fast adders like Carry Skip Adder (CSA) and Carry Look-Ahead Adder (CLA) to increase the speed of operation.

Key Words: fast adders, Carry Select Adder (CSA), Modified Carry Select Adder (MCSA), Carry Skip Adder (CSA), Carry Look-Ahead Adder (CLA).SQCSA, Modified SQCSA.

1. INTODUCTION

In rapidly growing electronic industry, faster units are not only of concern for design but also smaller area and less power become major concerns for design of VLSI circuits. So a VLSI designer has to optimize area delay and power constraints for increasing portability and battery life of portable devices. As we know millions of instructions per second are performed in micro processors speed of operation is the most important constraint to be considered while designing multipliers. These constraints are difficult to achieve so depending on application compromise between constraints has to be made. There are many ways to design a adder. The Ripple carry Adder (RCA) exhibits the most compact design but slowest in speed because for an N-bit RCA, the delay is linearly proportional to N. Thus for large values of N the Ripple Carry Adder gives greater delay of all adders. An N-Carry Look-ahead Adder (CLA) gives fast results when compared to RCA for N ≤ 4, but for large values of N its delay increases. The structure of Carry Select Adder is built using dual Ripple Carry Adders which increase area. In order to reduce the area and power Modified Carry Select Adder(MCSA) is implemented where one ripple carry adder at each stage of addition is replaced with BEC (Binary to Excess-1 Converter).

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To further increase the performance of MCSA the other RCA's are replaced with still faster adders like Carry Skip Adder and Carry Look-ahead Adders long. The results show a greater improvement in terms of delay and number of logic levels is reduced. The square-root carry select adder is constructed by equalizing the delay through two carry chains and the block multiplexer signal from previous stage. It is also called as non-linear carry select adder. The existing modified SQRT CSLA uses Binary to Excess-1 Converter (BEC) instead of RCA with Cin-=1 to achieve lower delay and less area. The RCA with Cin=0 is also replaced with fast adders like CLA CSKA and CSA and analysis is done in terms of logic levels and delay.

2. PREVIOUS TECHNIQUES

Carry select Adder (CSA): Carry select Adder (CSA) is one of the fastest adders used in many data processors to perform fast arithmetic functions. The carry select adder partitions the adder into several groups, each of which performs two additions in parallel using dual RCA's. One copy evaluates the carry chain assuming the block carry-in is '0', while the other assumes it to be '1'. Once the carry signals are finally computed, the correct sum and carry-out signals will be simply selected by a set of multiplexers .The generic structure for a 16-bit CSA is shown below

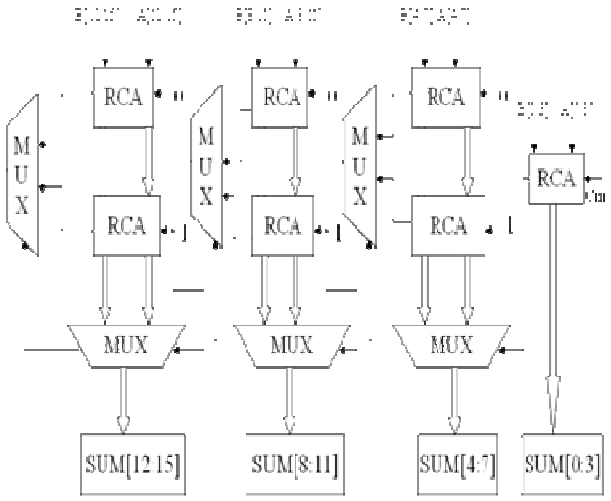

Fig1: 16-bit Carry Select Adder

An example for carry select addition with carry input '0' and carry-in '1' is shown below

```
          1010 1010 1011 1111
          0000 0011 1111 1010      (Cin=0)
          ---------------------------
(sum): 1010 1110 1011 1001
          ----------------------------
Cout='0'
          1010 1010 1011 1111
          0000 0011 1111 1010   (Cin =1)
        ---------------------------------
Sum:   1010 1110 1011 1111
          ---------------------------------
Cout='0'
```

Modified carry Select Adder (MCSA): In Carry Select Adder more area is occupied because of dual Ripple Carry Adders (RCA) and also carry-out at every stage must ripple. So in order minimize delay caused by one of the RCA whose carry input is '1' and to optimize area one RCA is replaced with Binary to Excess-1 Converter (BEC), by which gate count will be reduced by a very large amount and computational time is optimized when compared to rest of the adders as discussed above. A generic structure for 16-bit Modified Carry Select Adder is shown below.

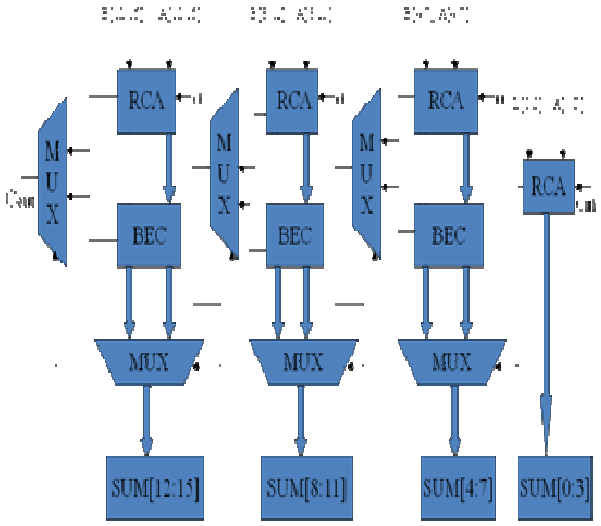

Fig2: 16-bit Modified Carry Select Adder

In the above architecture at each stage sum bits of RCA are given as input to BEC Instead of calculating sum with cin='1' using RCA. And the logic for BEC is shown below.

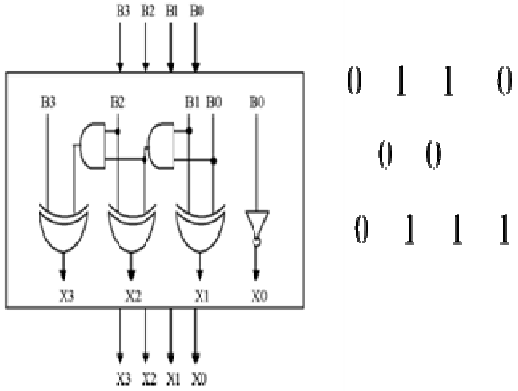

Fig3: Logic diagram of 4-bit BEC with example

Depending upon the carry out bit of the previous stage the sum is selected either from RCA or BEC with the help of 2x1 multiplexer's at each stage. An example of MCSA operation is shown below by randomly considering input bit stream.

```
          1010 1010 1011 1111
          0000 0011 1111 1010      (Cin=0)
          ---------------------------------------
Sum:      1010 1110 1011 1001

          1010 1110 1011  1111  (BEC)
             1      1      1    1010  (cin='0')
          ---------------------------------------
Sum:      1011 1111 1010   1111
```

From the above example we observe that even after replacing RCA's with carry input '1' with BEC there is no change in carry output and sum.

MCSA with CLA:

This architecture is similar to 16-bit Modified Carry Select Adder, the only change is that we replace Ripple Carry Adder with Carry Look-ahead Adder with Cin=1 along with BEC. As the delay of 4-bit Carry Look-ahead Adder is more when compared to 4-bit Carry Skip Adder.

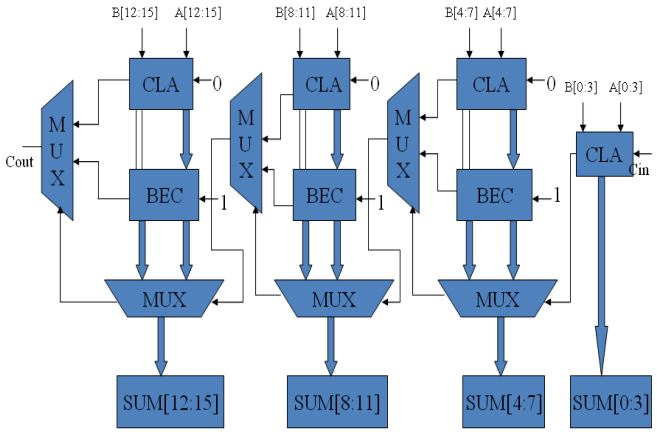

Fig1: 16-bit MCSA with CLA

MCSA with CLA:
As the delay in 4-bit Carry Look-ahead Adder is more when compared to 4-bit Carry Skip Adder because of that reason we are replacing 4-bit Carry Look-ahead Adder with 4-bit Carry Skip Adder in order to reduce the delay and power consumption with minimum speed penalty.

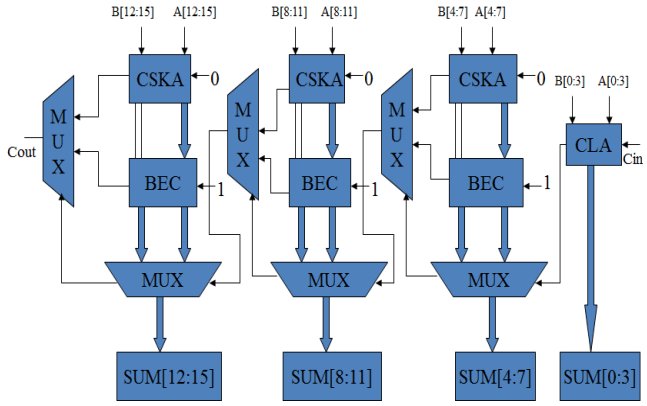

Fig1: 16-bit MCSA with CSA

Regular SQRT CSLA: The basic square-root Carry Select adder has a dual ripple carry adder with 2:1 multiplexer, the main disadvantage of regular CSLA is the large area due to the multiple pairs of ripple carry adder. The regular 16-bit SQRT Carry select adder is shown below

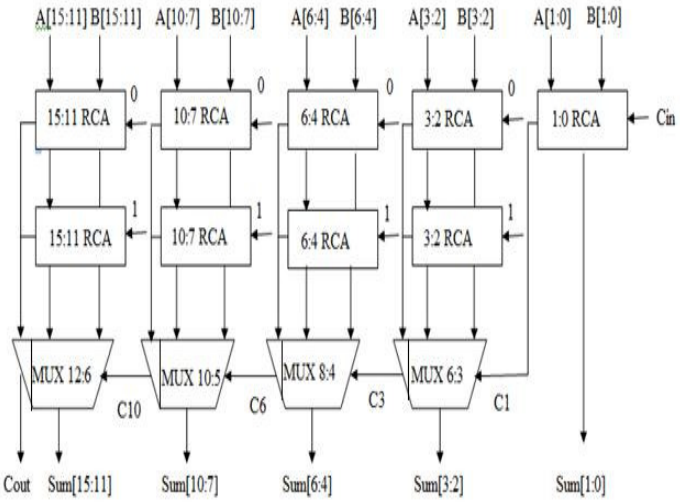

Fig1: 16-bit SQRT with CSLA

Regular SQRT CSLA with BEC:
The modified 16-bit SQRT CSLA using BEC is shown in Figure below. The structure is again divided into five groups with different sizes of Ripple carry adder and BEC The parallel Ripple carry adder with Cin=1 is replaced with BEC. One input to the multiplexer goes from the RCA with Cin=0 and other input from BEC. Comparing the individual groups of both regular and modified SQRT CSLA, it is clear that the BEC structure reduces delay. But it is clear that ripple carry adders still result in carry propagation delay.

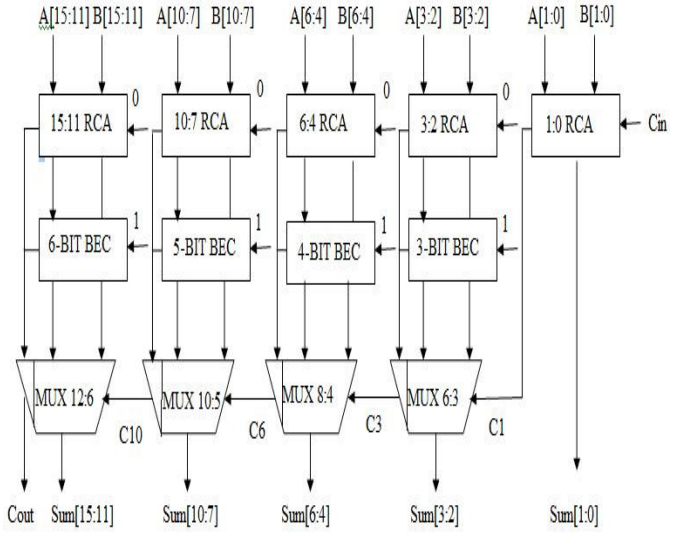

Fig1: 16-bit Modified SQRT with BEC

3. WORK DONE

For designing more area and speed efficient adder the Ripple Carry Adder in Modified Square root Carry Select Adder is replaced with fast adders. In order to know the efficient adder that can possibly replaced with RCA an analysis done on Modified SQRT CSLA by replacing RCA with CLA, CSKA, Carry save adder. The results are shown for all fast adders. First in MCSA the RCA is replaced with CLA and the waveforms are shown below. And from the synthesis report it is observed that area delay and logic levels are reduced.

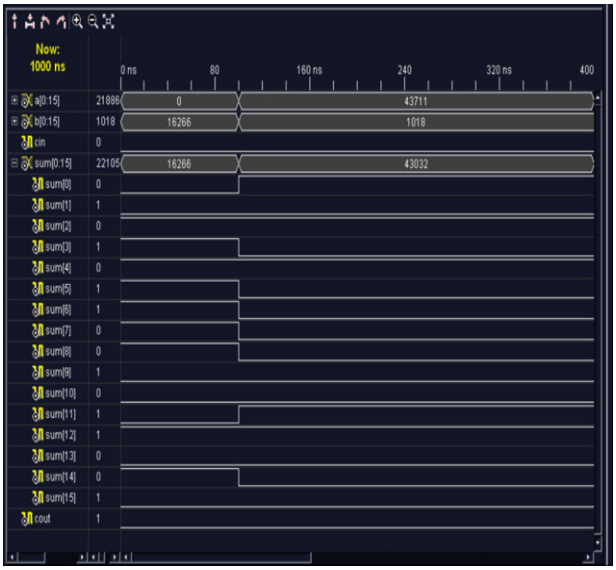

Fig8: Output waveforms of 16-bit SQRT MCSA with BEC

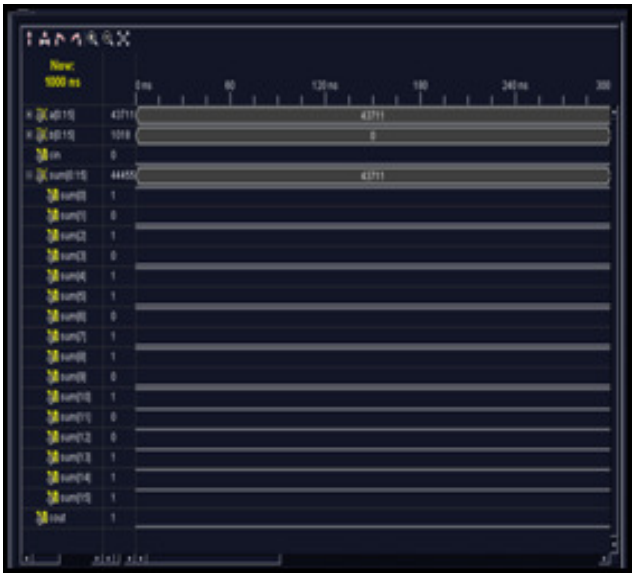

Fig9: Output waveforms of 16-bit SQRT MCSA with CSKA

It is observed that delay and number of logic levels for evaluation of final carry output are still reduced when replaced with CSKA compared with CLA. For getting further optimized results CSKA is replaced with Carry Save Adder and the waveforms are shown below.

Fig10: waveform of 16-bit SQRT MCSA with Carry save Adder.

The delay, number of logic levels for getting carry output and memory utilized by the addition operation using fast adders in MCSA is tabulated below. And it is inferred that SQRT MCSA with carry save adder gives better result.

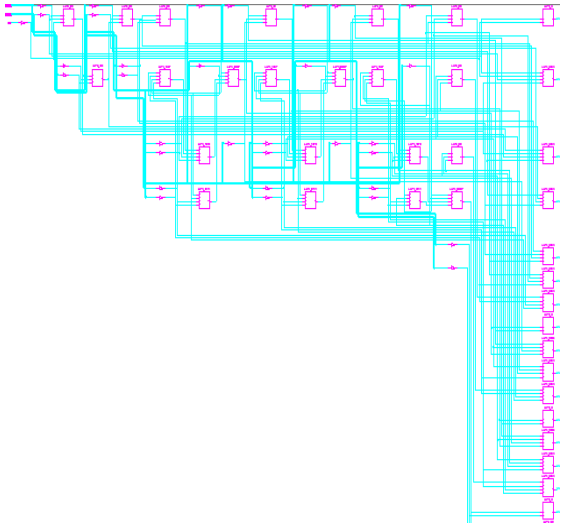

Fig10: Technology schematic of 16-bit SQRT MCSA with CSA

Table 6.1 Comparision of adders with delay, memory and logic levels

Adders	**Delay (nano seconds)**	**Memory (kilobytes)**	**Logic Levels**
Ripple Carry Adder	33.378ns (15.281ns logic, 18.097ns route)	177908	18
Carry look-Ahead Adder	31.744ns (15.281ns logic, 16.463ns route)	178228	18
Carry Select Adder(CSLA)	27.844ns (13.628ns logic, 14.216ns route)	178164	15
Modified Carry Select Adder	18.982ns (10.392ns logic, 8.590ns route)	141536	9
MCSA with CLA	18.458ns(10.514ns logic, 7.944ns route)	140512	9
MCSA with CSKA	14.367ns (9.029ns logic, 5.338ns route)	178484	7
Sqrt Carry Select Adder	26.540ns (13.147ns logic, 13.393ns route)	179508	14
Modified Sqrt Carry Select Adder	17.030ns (9.981ns logic, 7.049ns route)	180532	8
M-Sqrt CSA With CSKA	12.055ns (8.118ns logic, 3.937ns route)	188788	7
M-Sqrt CSA With CSA	10.042ns (7.031ns logic, 3.011ns route)	168728	6

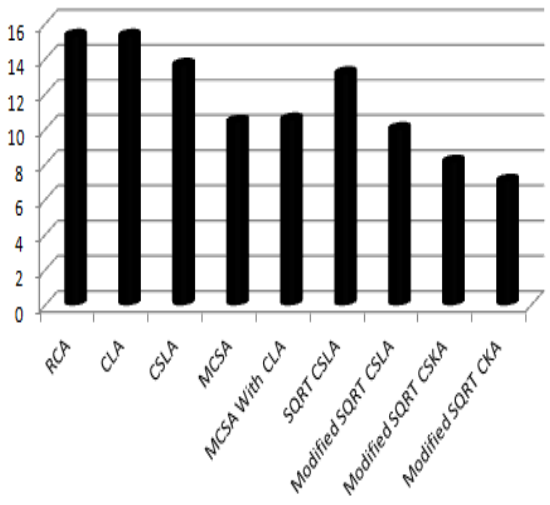

Fig11. Logical delay comparison of adders

4. CONCLUSIONS

In this paper three new architectures are presented for SQRT MCSA (Modified Carry Select Adder). Comparisons are made between different adders in terms of logic levels and delay. The proposed full adders show good performance and among the proposed SQRT MCSA's, MCSA with carry save adder show much optimized results.

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