Radiations On Static Random Access Memory Cell

Birinderjit Singh Kalyan

Abstract: With increased memory capacity usually comes increased bit line parasitice capacitance. This increased bit line capacitance in turn slows down voltage sensing and makes bit line voltage swing energy expensive resulting in slower more energy hungry memories. A full description of the various methods is beyond the scope of this article; instead, the focus is on providing primary developments that have taken place in the area of radiation effects on SRAM In this paper a comparision of different current mode sense amplifiers with flip flop structures using 0.35µm technology is presented with the effect of Radation effectv of 100 Krad exposures. Simulations results are given regarding sensing delay and power dissipation.

Keywords: BL, 0.35µm technology, S-R flip flops, SRAM, current sense amplifiers, Single event upset, Soft error rate, Total ionizing dose, Radiation effects, Single event transient

I. INTRODUCTION

Sense amplifiers are strongly related to the access time of memory, as they are used to retrieve the stored memory data by amplifying the small signal variations in the bit-lines. Designing fast, low power and robust sense amplifier circuits is a challenge. As SRAM [2],[3] chip density increases, the bit lines get longer and longer, resulting in increasing bit line capacitances. This capacitance creates a problem during reading of the cell data, since it will take a long time for the driver transistor of SRAM cell to discharge the bit line capacitance and create high power consumption as well, since bit lines need to be pre charged to $V_{DD.}$ Therefore to speed up the read time, sense amplifiers are utilized. Sense amplifiers compare the current or voltage of the bit line and its complement and amplify the difference between them to achieve faster access times. Current sensing scheme seems to be more reliable for realizing high speed and large size memories, as no large voltage swing on bit lines is needed. Current mode sense amplifiers sense the difference in the current on the bit lines and amplify the difference.

II. RADIATION SOURCES

The amount of radiation that semiconductor devices and materials encounter during their life cycle strongly depends on the radiation environment and their operating conditions. For space missions and military applications, it is obvious that there is a radiation-harsh environment. Cosmic rays, solar particle events, Van Allen radiation belts, nuclear reactors, nuclear explosions, secondary particles and radioactive impurities present in the chip packaging materials are the typical radiation sources. Alpha particles, which are capable of ionizing Si by generating EHPs, are emitted by radioactive impurities that are present in the integrated circuit (IC) package and in the IC itself.

- *Birinderjit Singh Kalyan*
- *Electronics and Communication Department, SVIET, Banur.*
- birinderjit@msn.com

III. ANALYTICAL MODELING OF IRRADIATED DEVICE

The Compact models are needed to compute analytically the device characteristics, rapidly enough, for use in circuit simulators to design and optimize the performance of ICs. The analysis and modeling of the "soft failures" was published by Kirkpatrick *et al*. [14] developed formalism for modeling the diffusion and collection of charge from ionizing particles in Si; it was followed by another approach that considered some of the details of radiation interactions with ICs. [15] This program formed cornerstone of the cosmic ray SER modeling program. [15] Zoutendyk *et al*. [16] developed empirical model of SEU for NMOS depletion load SRAM. Geometry-dependent analytical method for predicting upsets for 3-µm CMOS bulk asymmetric SRAM was developed [17]. A SPICE based analysis for SEE had been reported [18],[19],[20],[21].

Figure 1 and Figure 2 show that significant off-state leakage current is observed when devices are irradiated. Recently, an analytical model for irradiated FinFET device has been reported [29]. This model can be used to predict the shift in threshold voltage, mobility degradation, drain current and sub-threshold leakage current in irradiated FinFET device.

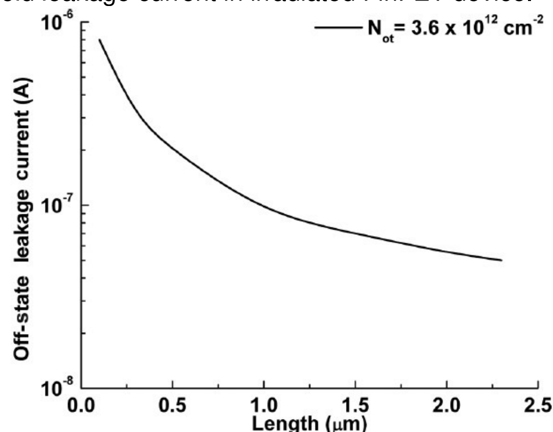

Figure1: Off-state leakage current for traps [27].

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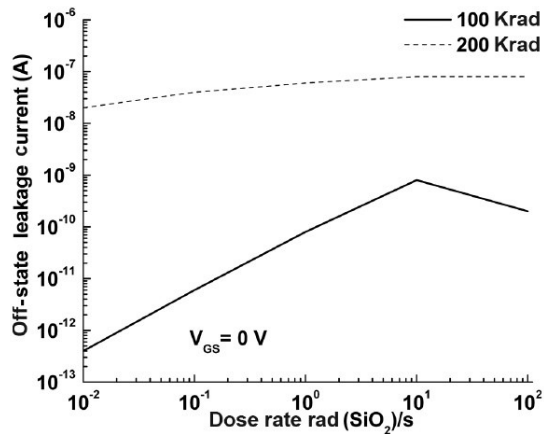

Figure2: Off-state leakage current against dose rate [28].

The modified cell architectures have been developed to make SRAM cell less sensitive to charge deposited by particle strike. The first popular solution proposed for SRAM designs is the Whitaker cell. It has a connection of transistors such that in no condition a transient in one of the vulnerable nodes can propagate, as shown in Figure 3. Another solution that was extensively used to harden SRAM cells in old technologies is the addition of two large resistors to the cell loop [30]. The function of the resistors is to delay the propagation of the signal across the loop. However, the speed penalty it introduces is incompatible with the performance of advanced SRAM circuits. Hite *et al*. [31] implemented 256 kB SRAM with transistor resistor cross coupling to increase radiation hardness as shown in Figure 4. For 1-µm, 256-kB SRAM, SEU immunity of less than 1×10^{-10} errors/bit-day was reported [31]..

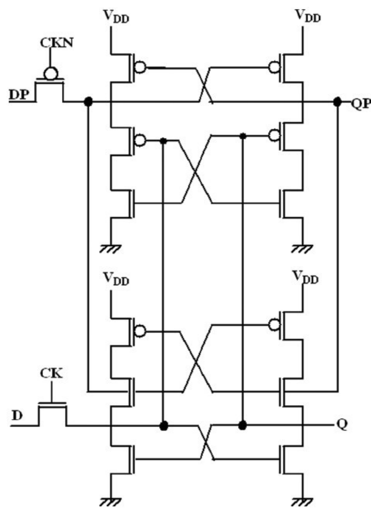

Figure 3: Low-power SEU immune SRAM cell.

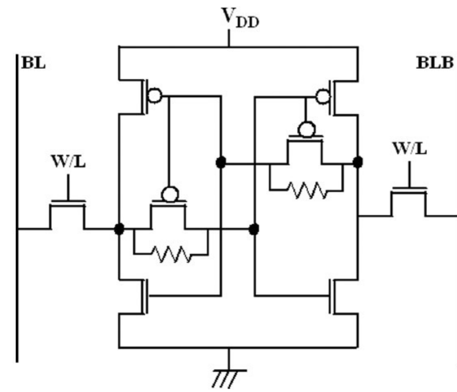

Figure 4: SEU immune SRAM cell [31].

The architecture reported in literature is Dual Interlock Cell (DICE) [32] which has been used in real applications. As shown in Figure 4, DICE cell consists of a symmetric structure of four CMOS inverters, where each inverter has the n-channel transistor and p-channel transistor, separately controlled by two adjacent nodes storing the same state. The four nodes of the DICE cell form a pair of latches in two alternate ways, depending on the stored logic value. The advantages of the DICE include low transistor count, no static power consumption, and rapid recovery time. In addition, the latch does not depend on specific transistor ratio and process parameters in order to function properly. Also, DICE latch design does not upset when a single node collects charge, but upsets when multiple nodes collect charge.

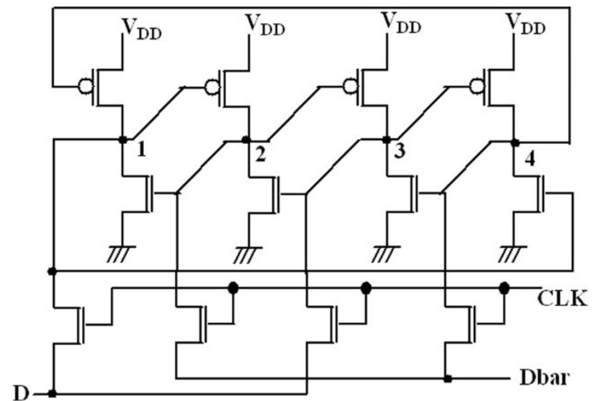

Figure: 5 DICE latch [32]

IV. SIMULATION AND EXPERIMENTAL RESULTS

The simulation results are based on the 5V/0.35µm CMOS technology. Comparison tables of different current sense amplifiers and flip-flop structures are presented with the impact of radiation.

V. COMPARISON OF DIFFERENT CURRENT SENSE AMPLIFIERS OF SRAM

Table 1: Comparison of different current sense amplifiers

Type of C.S.A	Delay(ns)	P_D(mw)	Clocking signals	No. of Tx's
Clamped	3.4	12.0	3	9
Latch	4.6	0.22	1	9
Izumikawa	4.2	0.45	2	7

Table 2: Comparison of S-R F/Fs

Type of C.S.A	Delay(ns)	P_D(mw)	No. of Tx's	Radiation (Delays)
Nikolic	3.8	2.5	16	5
Kim	3.8	6.7	14	5
Rubil	9.7	2.0	10	12
Stroll	9.3	2.3	12	12

Table 3: Overall result

Type of C.S.A	Delay(ns)	P_D(mw)	No. of Tx's	Radiation (Delays)
Latch+Nikolic	3.65	3.8	25	6.75
Latch+Kim	7.15	3.8	23	8.67
Latch+Rubil	2.45	9.7	19	9.33
Latch+Stroll	2.75	9.3	21	9.45

VI. CONCLUSION

A comparative study of various current mode sense amplifiers has been carried out in 0.35µm CMOS technology with the impact of 100 Krad raditions on SRAM and sense amplifiers. We conclude that Nikolic with latch sense amplifier performs better in terms of power dissipation and speed without radiation, when the 100krad is introduced the simulations the delay increases. The delays increase due to the introduction of extra ions in the device which make the memory more inefficient to work in radiated environment. Simulation results are shown in the above tables as well as in form of waveforms as mentioned below.

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