Non-Isolated Three Stage Interleaved Boost Converter For High Voltage Gain

Arundathi Ravi, A.Ramesh Babu

Abstract: In this paper, three stage high step-up interleaved boost converter with voltage multiplier cells(VMCS) and three state switching cells(3SSC) is proposed. The new method has been examined under various scenarios, including the loss of switches, ripples and stress. In the proposed topology an additional stage of voltage multiplier i.e, three stages is added which will increase the voltage gain and efficiency, reduces switching and conduction loss, voltage and current stress across switches and ripples. Another important feature of this converter is the lower blocking voltage across the controlled switches compared to similar circuits, which allows the utilization of MOSFETs switches with lower conduction loss. The simulation of proposed converter was done using MATLAB and the stimulation result was validated.

Index Terms: voltage multiplier cell, interleaved boost converter, high voltage gain, efficiency, power factor correction, state switching cell, Electro magnetic interference.

I INTRODUCTION

Dc-dc converter is a device which produces a dc output voltage when an dc input is given. If output voltage needed is higher than input voltage we go for boost converter. The conventional boost converter can be used for step up applications because of low conduction loss, simple structure and low cost [1]. However, it is not suitable for high step-up applications. The requirement of extreme duty cycle to obtain high voltage gain is a major limitation. In order to remedy these problems, use of low frequency or high frequency power transformers [2] have been suggested. However, there exists a need for galvanic isolation between the input and output stages of the power converters. To obtain high voltage step-up converters non isolated converters with large conversion ratios [3] are proposed, where multiple stages are connected in parallel but this will lead to high component count. In applications where dc isolation is not necessary, a transformer would normally be required for large voltage conversion ratio. However, leakage inductance of the transformer causes some problems as switch voltage overshoot, EMI generation and energy dissipation in snubbers. Hence a boost converter using switched capacitors is proposed [4], where high voltage gain can be obtained, but it is restricted to low power applications. Also large number of capacitors was used and as the multiplier was connected in the high-voltage (output) section of the converter (after the boost section), the diodes were submitted to voltage stress. Another topology which consists of clamp mode coupled-inductor [5] boost converters operating with the advantages of high voltage gain ratio and half output voltage stress across the switches.

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As disadvantage, it can be pointed out the pulsating input current and the high current stress through the clamping capacitor Cc. Next step was cascading one or more boost converter [6] to obtain high gain. The main drawbacks in this case are increased complexity and reverse losses, with consequent low efficiency and high electromagnetic interference levels. However, most require many switch blocks, which results in cost increase or reliability degradation. A new isolated dc-dc boost converter using [7] three state switching cell is proposed but the main drawback here is the increased complexity of the Auto-transformer construction. The influence of the leakage inductance shall also be taken in consideration in the design procedure. Several boost voltage-doubler [8] topologies have been introduced. However, the topologies described in [8] are not suitable for PFC applications in universal-input computer/telecom power supplies since they require the PFC stage output voltage to be at least twice that of the maximum line voltage, i.e., approximately 800 V. This increased voltage at the output of the PFC front end puts undue burden on the cost and performance of the downstream dc/dc converters. The use of voltage multiplier of cells [9] is not new and has already been reported in literature. For instance, the work developed in [9] employs multiplier capacitors to achieve high voltage gain. A single switch is used, while high voltage and high current stress result. As it was mentioned before, the use of the 3SSC may be interesting for high-power high-current applications. The converter studied in [10] uses two boost topologies coupled through an autotransformer with unity turns ratio and opposite polarity so that the current is equally shared between the switches. Moreover, voltage doubler characteristic is achieved. Even though the current stress through the switches is reduced, their voltage stress is less than or equal to half the total output voltage. Isolated drive circuitry must also be employed in this case. Converters with magnetically coupled inductance such as fly back or SEPIC can easily achieve high voltage gain using switches with reduced on-resistance, even though efficiency is compromised by the losses due to the leakage inductance [11]. An active clamping circuit is able to regenerate the leakage energy, at the cost of increased complexity and some loss in the auxiliary circuit [12]. In [13] there are two typical configurations of a grid-connected PV system i.e. single or two stages. The presence of several power stages un-determines the overall efficiency, reliability, and

compactness of the system besides increasing the cost. The major disadvantages of the high-step-up converters with an inductor [14] and a switched capacitor are the large switching losses due to the hard-switching operation. In addition, the numbers of the magnetic components are large, which limits the power level improvements. A significant drawback of [15] is high voltage stress across the semiconductors, so that it is not possible to employ switches rated at lower voltages, which are more efficient and less expensive. To remedy these problems, the proposed converter is introduced. The proposed converter in this work is based on the three state switching cell (3SSC) and voltage multiplier cell cascaded to produce the high voltage gain. The topology is shown in Fig. 1. Compared to the conventional converter, the proposed converter presents the following advantages: the 3SSC allows the utilization of only one primary winding; less copper and magnetic core are involved during the transformer assembly; and the moderate leakage inductance of the transformer allows the reduction of the commutation losses of the switches. The autotransformer of the 3SSC has small size, because it is designed for half output power of the converter and for a high magnetic flux density since the current through the windings is almost continuous with low ripple. Here the boost converter is interleaved as a result reduction of input output current ripples are observed. In addition to the advantages mentioned above there are few more merits, because of the increased number of stages. The merits are: input inductor operates with the double of the switching frequency, allowing weight and volume reduction; the voltage stress across the switches is lower than a half output voltage. The lower voltage across the switches allows the use of low on resistance MOSFETs, improving therefore, the efficiency. The proposed converter is capable of operating in high power and high frequency applications such as electric vehicles, uninterruptible power supplies, fuel cells, and photovoltaic systems.

2 PROPOSED TOPOLOGY

The main circuit diagram of proposed dc-dc converter with 3 state switching cell and voltage multiplier cells is shown in fig 1.

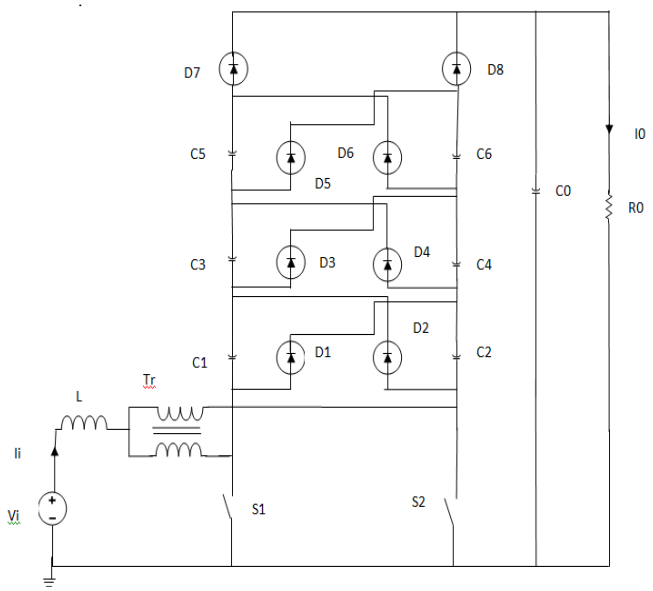

Fig.1. Proposed converter

In this circuit diagram there are voltage source V_i, storage inductor L_1, autotransformer T, two controlled switches (MOSFETs) S_1 and S_2, multiplier cells formed for diodes D_1, D_2, D_3, D_4, D_5, D_6, C_1, C_2, C_3, C_4, C_5, C_6, rectifier diodes D_7, D_8, output capacitor C_0, and load resistor R_0. Since three state switching cells are used, the current rating of switches can be reduced and at the same time this circuit can be used for high power and high current application.

3 MODES OF OPERATION

During a switching period Ts the operation of the proposed converter is divided into four modes. This is illustrated in Fig.3.

3.1 Mode 1

In this mode power switches S_2 and S_2 are turned ON, while all diodes are reverse biased. Energy is stored in inductor *L*, and there is no energy transfer to the load. The output capacitor C_0 provides energy to the load. This stage finishes when switch S_1 is turned off and is represented in Fig.3.a. The differential equation during this interval is given by

$$L\frac{di_{L1}}{dt} - V_i = 0 \qquad (1)$$

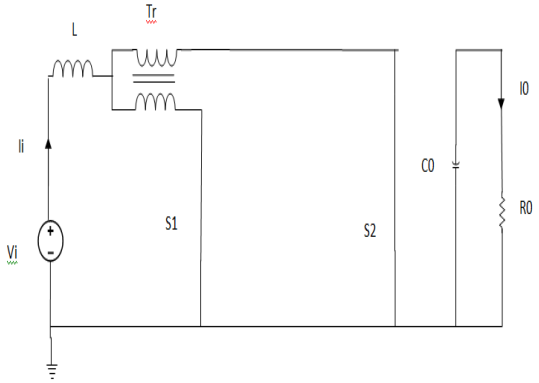

Fig.2 (a) Mode 1

3.2 Mode 2

The diodes D_3 and D_7 are directly biased, the energy of the inductor and source are transferred to the capacitors C_1, C_2, C_3, C_4, C_5 and for the load also. It is finished when the diode D3 is reversed biased. This stage is represented in Fig. 3©.

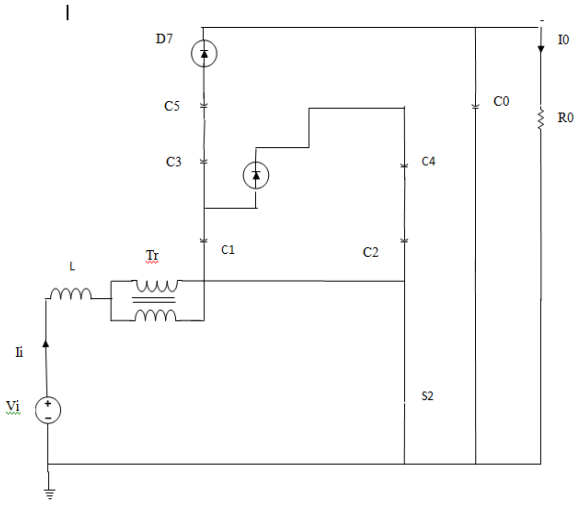

Fig.2 (b) Mode 2

3.3 Mode 3

Switch S1 is turned on and switch S2 is turned off diode is forward biased. The energy stored in the inductor in the first interval, as well as the energy from the voltage source are transferred to the capacitors C1, C2, C3, C4 and C5. This stage is represented in Fig. 3.c. The differential equation during this interval is equal to

$$L\frac{di_{L1}}{dt} + \frac{I_{L1}}{2C_{eq}} - V_i = 0 \qquad (2)$$

L_i- storage inductor
V_i- input source voltage
C_{eq}-Equivalent capacitor

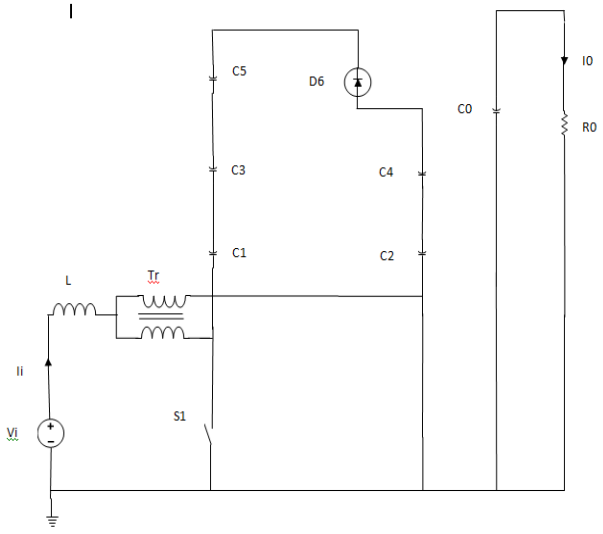

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Fig.2 (c) Mode 3

3.4 Mode 4

The diode D_2 is directly biased and the energy of the inductor and source are transferred to the capacitors C_1, C_2, C_4, C_6 and also for the load. This stage is finished when the diode D_2 is reversed biased. This stage is represented in Fig. 3.d.

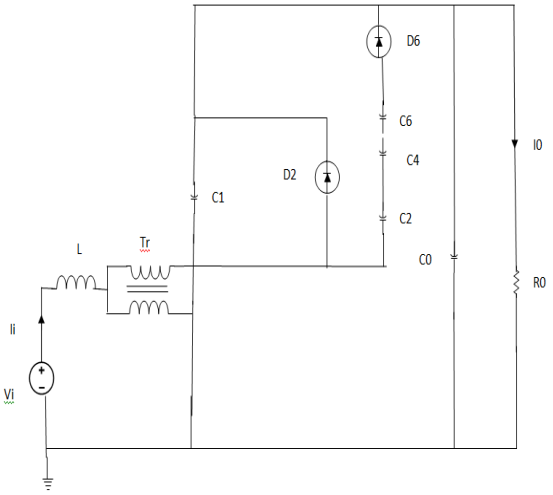
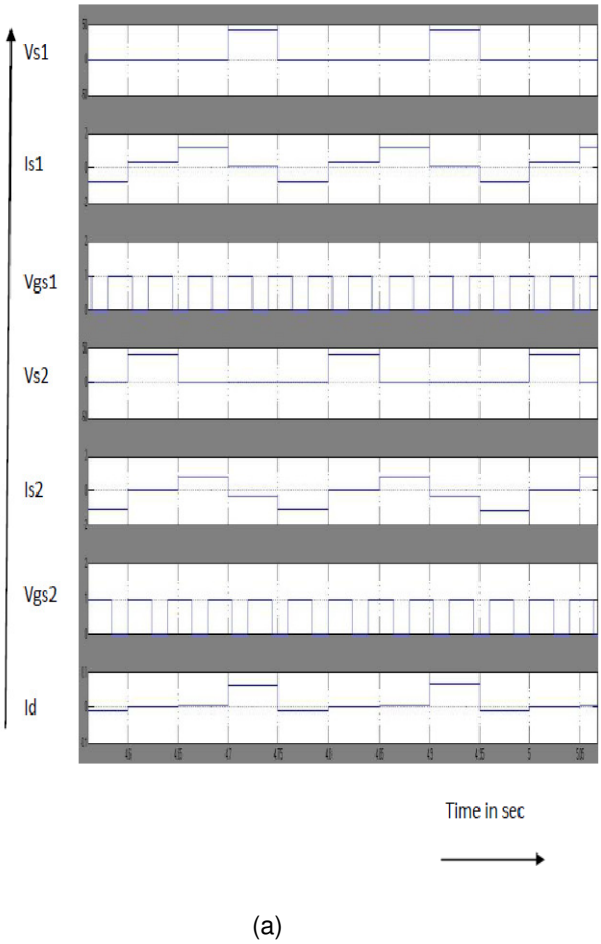


Fig.2 (d) Mode 4

4 KEY WAVEFORMS



(a)

Fig.3. Waveforms of Gate pulse, Voltage and Current across (a) switch 1 and switch 2

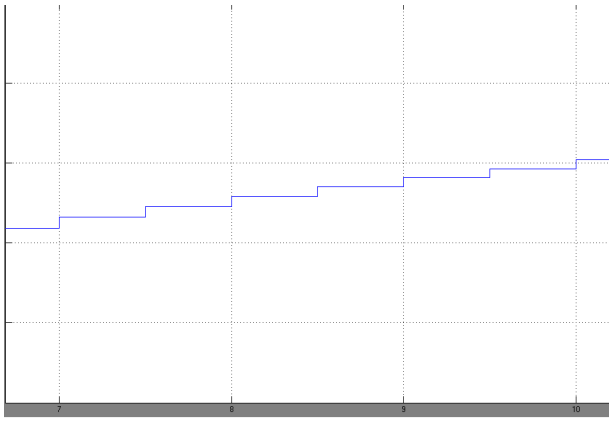


Fig.4. Inductor current

As it seen from the waveform the inductor current is keep on increasing.

5 DESIGN EQUATIONS

The value of magnetizing inductor L can be design based on the equation

$L= V_o/(16*f_s\,(mc+1)*\,\Delta I_L)$

The value of capacitor can be design based on the equation

$C= (1*I_i\,(1-D))/(3nfs*\Delta V_{cn})$

In the above equation input current, duty ratio are given by below equations.

$D=1-V_i/V_o$

$I_i= (I_o\,(mc+1))/(1-D)$

$C_0= (I_o\,(1-D))/(2*\Delta V_{c0}*f_s)$

In the output capacitor equation output current is given by below equation.

$I_o=V_o/R$

where V_o- output voltage, f_s-swiching frequency mc-voltage multiplier, ΔI_L-ripple current D-duty ratio ,I_o-output current, ΔV_{cn}-capacitor ripple voltage**.**

6 SIMULATION RESULTS

Simulation is done using MATLAB. MATLAB is a software package for computation in engineering, science, and applied mathematics. Simulink (Simulation and Link) is an extension of MATLAB by Math works Inc. It works with MATLAB to offer modeling, simulating, and analyzing of dynamical systems under a graphical user interface (GUI) environment. The following model has been created using SIMULINK. MATLAB offers a powerful programming language, excellent graphics, and a wide range of expert knowledge. This model contains dc voltage source, gate pulse circuit, power switch MOSFETS, inductor, capacitors, diodes and load. The table below shows the components list for the simulation circuit:

TABLE 1- PROTOTYPE PARAMETERS

COMPONENTS	VALUES
Input voltage	12 V DC
Output voltage	150 V DC
Input inductor L_1	10 *mH*
Capacitors C_1-C_4	2.2 μF
Output Capacitors C_0	44 *nF*
Output Resistor	1000Ω

Simulation circuits and stimulations result of output voltage waveforms are shown in Figs. In one stage circuit an input dc voltage of 12 V is given to the boost converter and output is stepped up to 90 V. Its input current and output voltage are shown below.

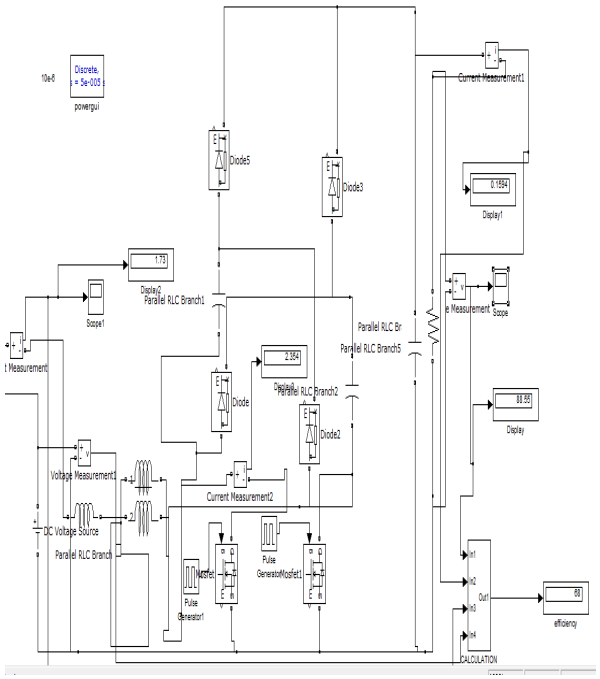
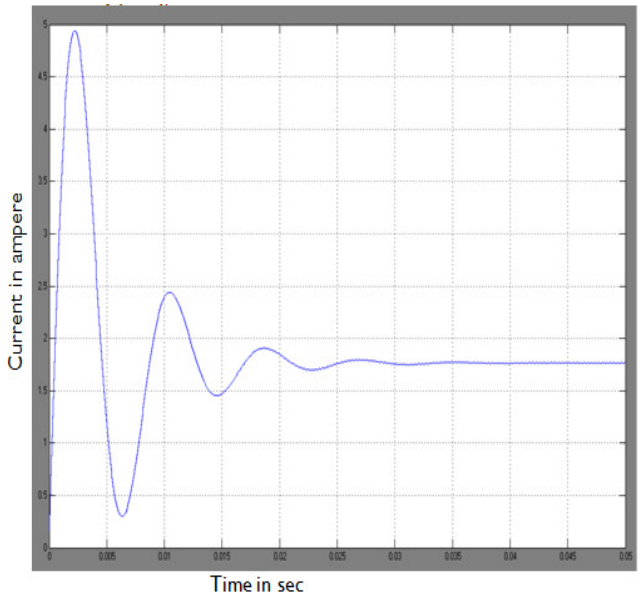
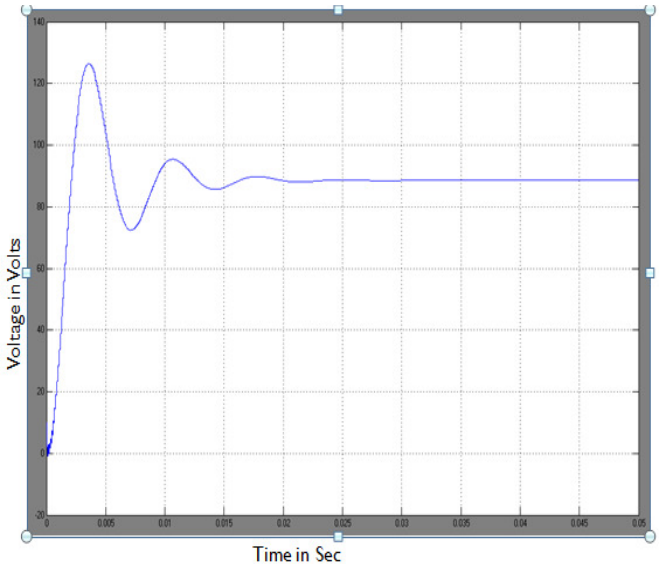


Fig.5. Simulation circuit for one stage



(a)



(b)

Fig.6. (a) Input current of one stage (b) Output voltage of one stage

In two stage circuit an input dc voltage of 12 V is given to the boost converter and output is stepped up to 110 V. Its stimulation circuit, output voltage and ripple current waveforms are shown below

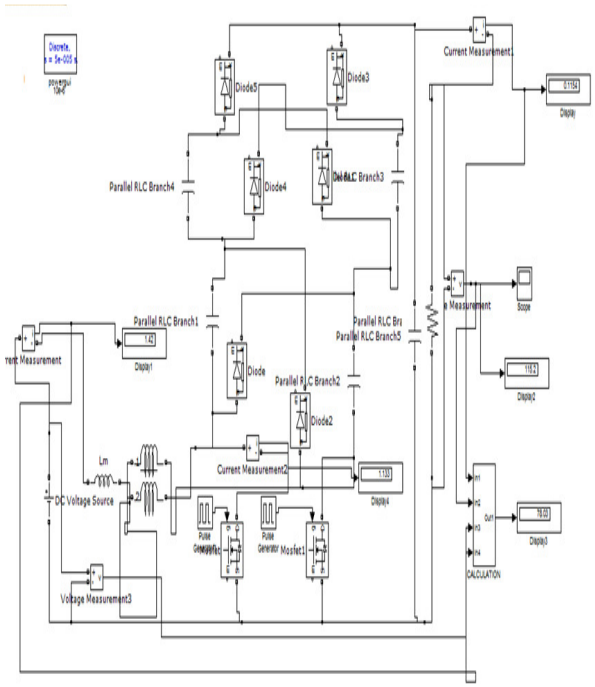
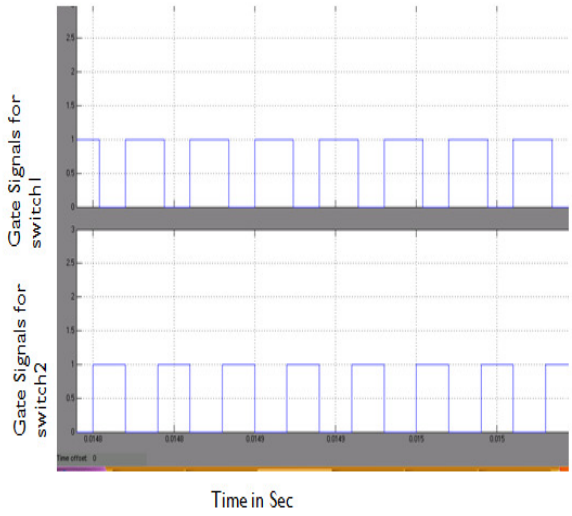
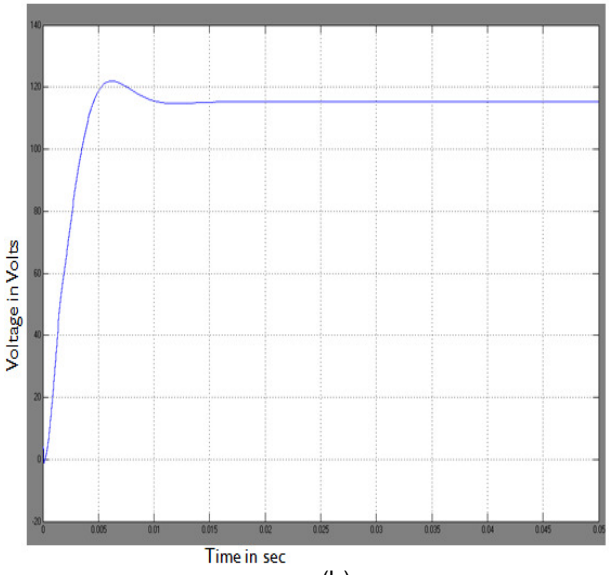


Fig.7. Simulation circuit for two stage



(a)



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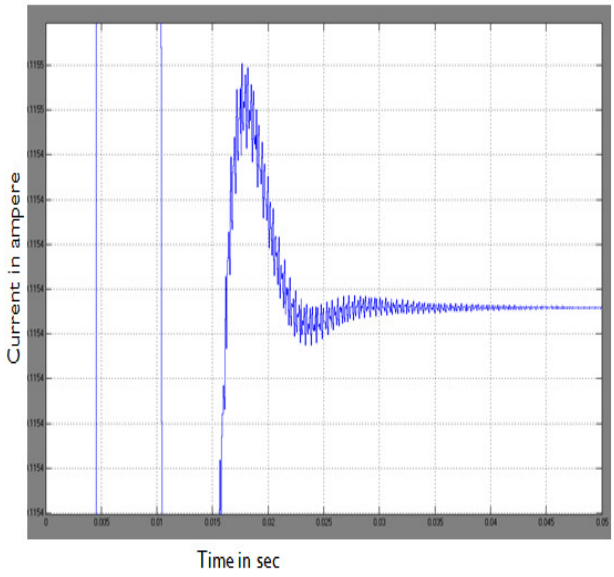


(c)

Fig.8. (a) Gate signals for the two switches, (b) Output voltage of two stage (c) Ripple current of two stage In three stage circuit an input dc voltage of 12 V is given to the boost converter and output is stepped up to 155 V. Its stimulation circuit, output voltage and ripple current waveforms are shown below

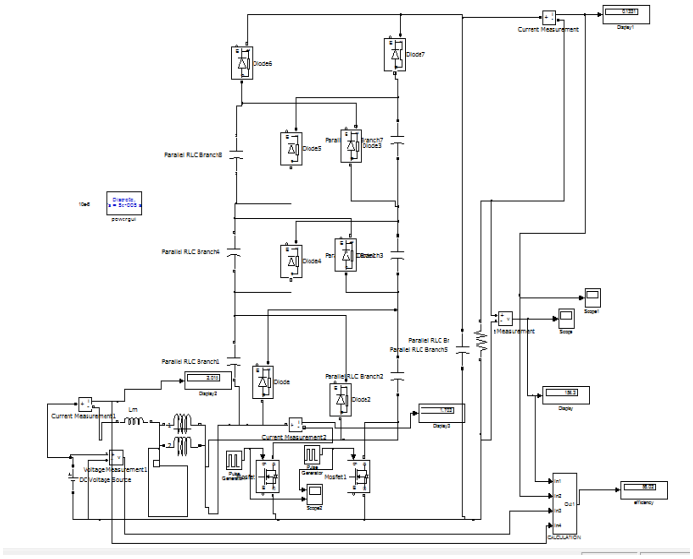
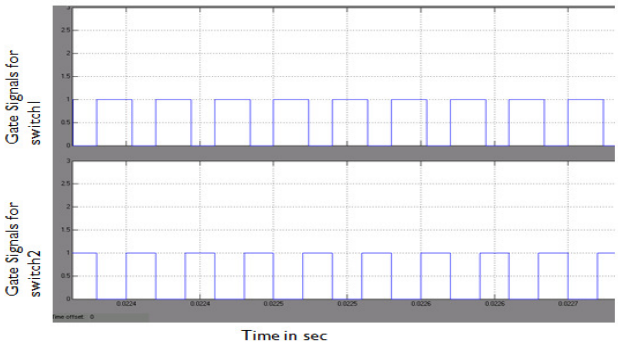
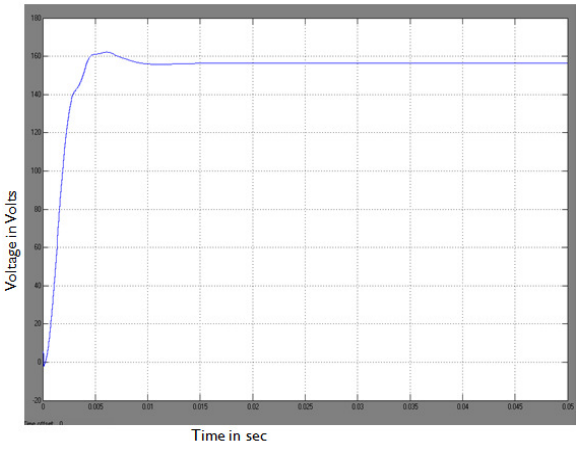


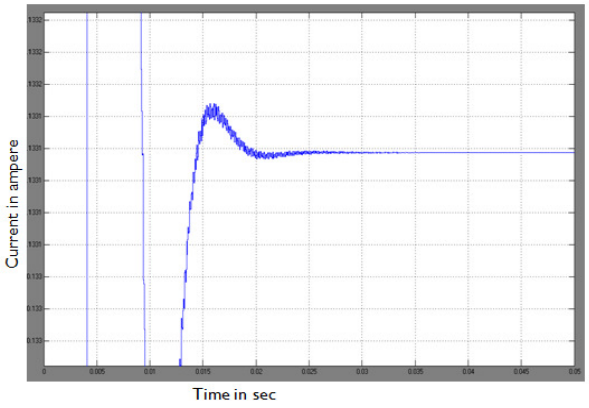
Fig.9. Simulation circuit for three stage



(a)



(b)



(c)

Fig.10. (a) Gate signals for the two switches, (b) Output voltage of three stage (c) Ripple current of three stage

7 PARAMETER ANALYSIS

- **Conduction Loss= Id^2*Rdson**

Conduction loss depends on the ON state resistance of MOSFET ($R_{ds(on)}$), which can be reduced by selecting a low $R_{ds(on)}$ MOSFET.

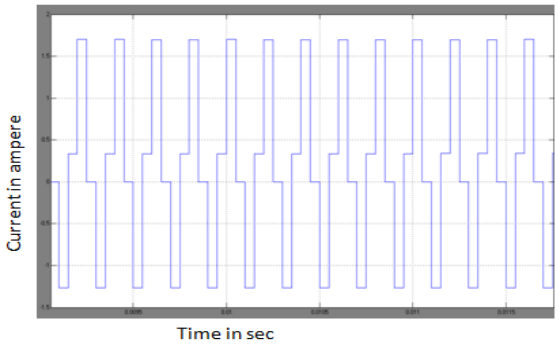


Fig:11: Drain current

- **Switching Loss= 0.5Vds*Id(Trise+Tfall)*Fsw**

The switching losses of the MOSFET are the loss across the switch during turn on and turn off instant.

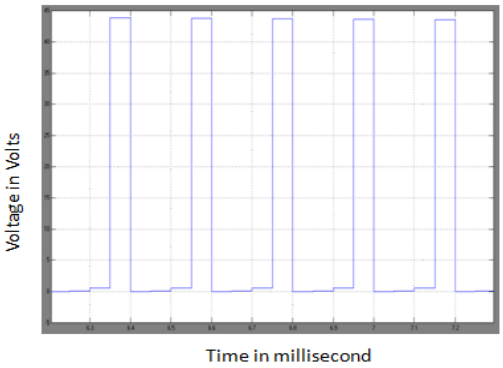


Fig: 3.11`: Voltage across switch when it is ON

- **Ripple current is calculated from the graph**

where Id = drain current, Trise = rise time, Tfall = fall time, Fsw = switching frequency, Vds = drain-to-source voltage, Id = drain current, Rdson = on state resistance of the mosfet

- **Total switch stress (S)=Peak Blocking Voltage(V)*Drain Current(Id)**

The peak blocking voltage is the voltage across the switch, when it is in OFF condition

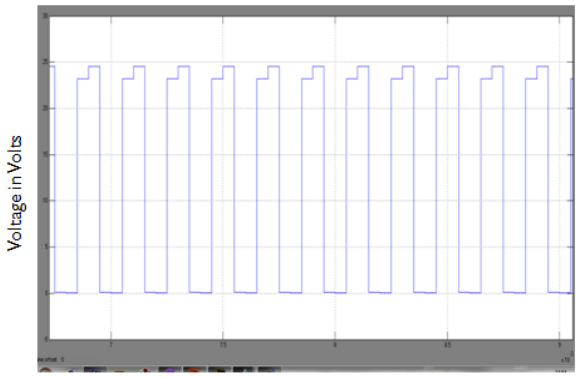


Fig.11. Voltage across an OFF switch

8 CONCLUSION

This project has proposed non isolated high voltage gain DC-DC converters where a comparative study of different stages is been (3.5) d observed that the output voltage, gain and efficiency are improved. An important characteristic that can be seen in this topology is the reduced current ripple, switching losses and the total stress across each switches. Also, the advantages of the 3SSC are also incorporated into the resulting topology. Finally, we can say that as the number of stages increases the output voltage get boosted there by increasing the efficiency. Hence the proposed converter can be used in high voltage applications such as fuel cell systems, photovoltaic systems and UPS. Other features that can be seen in the experimental results are the lower blocking voltages across the controlled switches compared to similar circuits, which allow the utilization of MOSFETs switches with lower conduction losses.

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