Analysis And Design Of Fir Filter Using Modified Carry Look Ahead Multiplier

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Abstract: The dynamic growth in portable multimedia devices and communication system has increased the demand for area and power efficient high-speed Digital Signal Processing (DSP) system. The Finite Impulse Response (FIR) Filter is the important component for designing an efficient digital signal processing system. Usage of digital Finite Impulse Response (FIR) filter is one of the prime block in DSP. Digital multipliers and adders are the most critical arithmetic functional units in FIR filters and also decides the performance of whole system. Thus, the low power system design has become a major performance goal. This paper proposes an FIR filter which is designed using Carry-Look ahead adder and multiplier. Where the multiplier is proposed by internal circuit of Modified Carry Look ahead Adder. Carry-Look ahead Adder (CLA) is used for addition operation which uses fastest carry generation technique to increases the speed by reducing the time required to fix carry bits and multiplier performs multiplication process in a hierarchical manner. Thus, the proposed method can minimize the active power and delay of the FIR filter. The tentative results shows that the FIR filter using proposed multiplier method achieves less amount of delay and power reduction compared to conventional method. The proposed FIR filter is programmed using Verilog code and was synthesized and implemented using Xilinx ISE 14.7 tool, and the power is analyzed using Xpower analyzer.

KEYWORDS: Carry Look Ahead Adder, FIR Filter, Multiplier, Digital Signal Processing

I INTRODUCTION
Optimized design of digital logic systems is one of the most essential part of VLSI system design [1]. In modern era, a significant range of research work is carried out sprouting efficient architectures to reduce the complexity of DSP system. Digital FIR filter is the fundamental arithmetic operation used in most of the communication system and in various signal processing devices [12]. Digital FIR filter performs lot of arithmetic and logical operations that are extensively used for signal analysis and estimation, selection of band for the computation and signal preconditioning etc. Especially, it requires more rapid calculations for updating their filter coefficients [3]. In general, the longest critical path delay of the FIR filter mainly focus based on the computation time required for the multiplication and addition operation. Multipliers and Adder are the key hardware blocks of FIR filter which contributes in reduction of chip area, power and delay for each operation [2]. First considering the multipliers in FIR filter having long latency, large area and consume considerable amount of power. Therefore the main goal is to attain high speed and low power consumption multiplier. Second, CLA is used for addition operation which improves the speed by decreasing the total time necessary to fix the carry bits. This paper deals with the implementation of FIR filter with modified multiplier based on the CLA [9]. The performance of the proposed FIR Filter are compared in terms of area, delay and power using the conventional and modified technique. The paper is structured as follows, Section II presents the concepts of FIR filter. Section III details with the basic carry look ahead adder technique. Section IV gives the proposed FIR filter using modified multiplier based CLA, Section V performs simulation results and comparative analysis, Section VI provides Conclusion.

II FIR FILTER
In this segment, the basic theoretical concepts of direct form realization of FIR filter is discussed. The FIR filter can be obtained using linear convolution which simply performs the convolution operation between the given input signal and the fixed filter coefficients. The basic representation of an FIR filter is given by equation 1

\[ y(n) = \sum_{k=0}^{N-1} b_k x(n-k) \]

Where \( y(n) \) is the output response, \( x(n) \) is the input signal, \( M \) is the order of the filter and represents the filter coefficients for the \( M \) tap FIR filter. The below figure 1 shows the structure of a direct form \( M \)-tap FIR filter with length \( N \). The input of the FIR filter \( X_n \) is given to the delays of the direct form structure. In this structure the \( b_n \) values are the coefficients of the operation and are designed to the multiplication of the samples. The output at time \( n \) is the summation of the delayed samples multiplied by the appropriate samples. The process in which selecting the filter coefficients and length of the filter is called Filter Design.

![Figure 1: Direct form realization of M-tap Filter](image)

For the instance consider the filter having input sequence \( x(n) = [0,1,2,3,...,N-1] \) with the length of \( N \) and impulse response \( b(n) = [0,1,2,3,...,M-1] \) with the length of \( M \). Now performing linear convolution of \( x(n) \) and \( b(n) \) produces the

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output sequence \( y(n) \) and the length of \( y(n) \) is \( S = N + M - 1 \) (2) By adding required number of zeros to the input sequence and impulse response, the length of \( x(n) \) and \( b(n) \) can be made equal to \( S \). This process is recognized as zero padding process. The total length \( S = N + M - 1 \) can be obtained by increasing the length of \( n \) by \( N \) points and length of \( h(n) \) by \( M \) points. Both the sequences \( n \) and \( b(n) \) are finite in FIR filter, based on this sequences the linear convolution is also said to be finite. The output sequence \( y(n) \) is derived from the convolution operation of input \( x \) of length \( N \) with filter coefficient \( b \) of length \( M \). So the output sequence \( y(n) \) is given as follows,

\[
y(n) = \sum_{i=0}^{M-1} b(i)x(n-i)
\]

By expanding the Eq. (2) the direct form structure of FIR filter is designed.

\[
y(n) = b(0)x(n) = b(1)x(n-1)+b(2)x(n-2)+b(3)x(n-3)+ \ldots +b(M-1)x(n-M+1)
\]

This construction of direct form structure is also said as canonical structure meanwhile the number of delay blocks present in the architecture is equivalent to the order of difference equation that contains \( M-1 \) delay blocks, \( M \) multiplications and \( M - 1 \) additions.

### III CARRY LOOK AHEAD ADDER (CLA)

Carry Look ahead algorithm speed up the operation to perform addition, because in this algorithm the carry for the next stages of process is calculated in advance based on the input signals given to the adder. The CLA exploits the fact that the carry generated by a bit-position depends on the three inputs to responding that position. If ‘X’ and ‘Y’ are two inputs then the function \( X=0 \) and \( Y=1 \), a carry is generated independently of the carry from the previous bit position and if \( X=Y=0 \), no carry is generated. Similarly if \( X \neq Y \), a carry is generated if and only if the previous bit-position generates a carry. ‘C’ denotes the initial carry bit of adder, “S” and “Cout” are said to be output sum and carry of the adder respectively. Then the Boolean expression for calculating next carry and addition in carry look ahead adder is :

- \( Pi = Xi \oplus Yi \quad \text{-- Carry Propagation} \quad (1) \)
- \( Qi = Xi \cdot Yi \quad \text{-- Carry Generation} \quad (2) \)
- \( Ci+1 = Gi + (Pi \text{ and } Ci) \quad \text{-- Next Carry} \quad (3) \)
- \( Si = Xi \oplus Yi \oplus Ci \quad \text{-- Sum Generation} \quad (4) \)

Thus, for 4-bit adder, we can extend the carry bit, as shown below:

- \( C1 = G0 + P0 : C0 \quad (5) \)
- \( C2 = G1 + P1 \cdot C1 = G1 + P1 \cdot G0 + P1 \cdot P0 \cdot C0 \quad (6) \)
- \( C3 = G2 + P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot P0 \cdot C0 \quad (7) \)
- \( C4 = G3 + P3 \cdot G2 + P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0 + P3 \cdot P2 \cdot P1 \cdot P0 \cdot C0 \quad (8) \)

### IV FIR FILTER DESIGN

Carry Look Ahead Adder is a kind of fast adder used in digital logic circuits. The CLA computes all the carry bits before the sum, which decreases the delay time to calculate the result of the larger value bits. The CLA solves the carry delay problem by predetermination of the carry signals in advance to the basis of the input signals. This technique was contrasted with the slow adder like RCA, where the adder should wait for the previous carry to generate the specific result and carry bits. The CLA uses additional circuitry to generate carry bits in parallel, which eliminates time required to calculate the larger value bit result. The architecture of 4-bit CLA is shown in Fig. 2. CLA can be separated as two segments: Partial Full Adder (PFA) and the Carry Look-ahead Logic. The PFA produce propagate signals \( pi \), generate signals \( gi \) and the sum output \( si \) and the carry-out bits \( ci +1 \) was generated by the look ahead logic circuit. The structure shows that Propagate \( P \) and generate \( G \) in a partial full-adder depends on the input bits only, the carry generator also not depends on its previous carry-in. As a result, once \( C0 \) is computed, \( C4 \) can reach stable state it does not want to wait for \( C3 \) to propagate.

#### Figure 2: Proposed carry-look ahead adder in Multiplier

The multiplier is proposed by internal circuit of Modified Carry Look ahead Adder which consist of four partial full adder with XOR gates and NAND gate. In Figure 2 it shows the partial products has been taken to generate and propagate signal. These generate and propagate signal has been used in look ahead section to generate carry. Here the carry is eliminated from first section and directly utilizing the propagate operation and generate to the input block of look ahead section. The FIR filter consists of three main components:

A D-FF to implement a simple delay. A Multiplier is used to implement the filter coefficients. An Adder to sum the nodes at the end of each tap. Functional verification of all the adders and multiplier are performed and these modified architectures are applied in 4-tap FIR filter finally results are summarized.
Here $X(n)$ is input filter coefficients and $B0, B1, B2$ and $Bn$ are transfer function coefficients and $Y(n)$ is output filter coefficient. Multipliers can be replaced with shift and add operation, that is MCM (Multiple Constant Multiplication) in which a set of constants (here $h0, h1, \ldots$) is multiplied with a variable (here $x(n)$). But the disadvantage in shift and add method is that the complexity and resource utilization is more. Another method is the use of transpose based structure.

V RESULTS AND DISCUSSION

A SIMULATION TOOL USED
Multiplier discussed above in this work is firstly designed using Xilinx 14.5 tool in Verilog HDL programming language. Different parameter like speed, power and delay of different multipliers are then analyzed.

B RTL VIEW OF CLA AND FIR
In CLA every bit in a binary sequence that to be added to the operation, the carry-look ahead logic will determine whether the bit pair will generate a carry or propagate a carry. This allows the circuit to "pre-process" the two numbers being added to establish the carry ahead of its time. Then, when the actual addition is performed, there is no delay comes out from the process when waiting for the ripple-carry effect operation.

C FIR
In FIR filter the result of the delay operates on the process of input samples. The values of $hn$ are the coefficients in which they are used for multiplication operation. So that the output reaches at time and the summation operation is delayed for all the other samples that are multiplied by the appropriate coefficients.

VI SIMULATION RESULTS
In CLA every bit in a binary sequence that to be added to the operation, the carry-look ahead logic will determine whether the bit pair will generate a carry or propagate a carry. The simulations result of existing adder with the proposed CLA adder are shown in the figure 6 and figure 7.
VII CONCLUSION

In this paper, the proposed design of digital FIR filter using modified multiplier based CLA is discussed. A basic analysis was performed in terms of area, power and delay. This multiplier based on CLA adder proved to be more efficient in terms of speed of operation compared to conventional multipliers. Based on the proposed multiplier, the architecture of direct form realization of digital FIR filter have been derived. The synthesis results show that the proposed FIR filter using modified multiplier based on carry look ahead adders achieves high speed and reduces the hardware cost with lesser power consumption related to conventional FIR filter with other multipliers. In future, the pipelining concept also extended to adder unit present in digital FIR filter to achieve better power and area reduction. Further the design of 16-tap FIR filter can be prolonged to n-tap that to be used in real time applications.

REFERENCES


