A Study On Test Pattern Generation Using Arithmetic Approach For Iscas 85 Benchmark Circuits

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Abstract: Test patterns are needed to test the functionality of integrated circuits. Most of the semiconductor industry depends EDA tool to generate patterns and are applied to the Circuit under Test (CUT) to check the functional verification of the circuit [1]. Those generated test patterns are insufficient in terms of (Test Application Time) TAT and Fault coverage. Important issues in testing is to detect more faults with minimized test patterns, reduce the test power and test application time. Test application time (TAT) is directly proportional to number of test patterns. An arithmetic approach is proposed to modify the test set in order to reduce the total test set. The test patterns of ISCAS 85 benchmark circuits has taken as reference for this work. Fault coverage and TAT are analyzed for each ISCAS'85 benchmark circuits. Experimental results shows that an arithmetic approach reduce the TAT without degrading the fault coverage.

Keywords: Test pattern Generation, Fault coverage, Test Application Time, Circuit under Test

1. INTRODUCTION

Very-Large-Scale Integration (VLSI) is the process of creating an Integrated Circuit (IC) by combining millions of transistors in order to get a single chip. VLSI began in the 1970s when complex semiconductor and technologies were being developed. The microprocessor is a VLSI device. The complexity of the circuit has been increased over years with the advancement of technology and testing of those circuits become complex and more important in order to prove the quality of product. The testing is done to check the functionality of the circuits after the verification process. Without testing and faults are detected in it, rectifying it at a later stage would be of no use. Circuits in test mode consume huge power compared to circuits in normal mode. The complexity of the circuits also increases the test power consumption. The test power also depend on the number of test sets. The reduction of test set also has an impact on test power. The organization of the paper is represented as follows. Section 2 discusses about basic need of testing, accumulator based test pattern generation methods its issues. Section 3 discusses proposed arithmetic approach Experimental works are discussed in Section 4 and Section 5 discusses the conclusion

2. TESTING

Testing helps to validate the quality of the chips in order to reduce the cost of testing by investigating the number of possible faults occurred in the Circuit under Test (CUT). Before assembling the chips into the systems every chip must undergo testing.

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If it's tested at the end of assembling as the whole product the cost of testing will be ten times as much at chip level. In order to detect the failures testing must be done. The role of testing is to detect the fault i.e., when something went wrong and the role of diagnosis is to find what went wrong exactly. With the growth of device counts and limited space conventional testing approach is not sufficient. The following figure 1 illustrates the basics of testing.

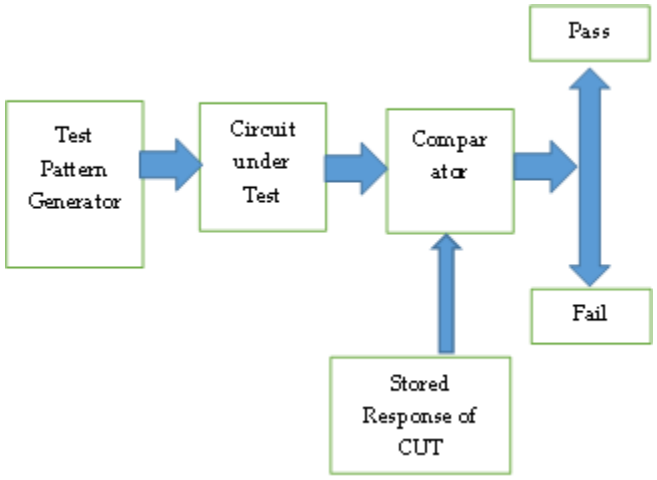

***Fig.1**. Testing of CUT*

Test pattern generator generates the test patterns. The generated test patterns are applied to Device or circuit that needs to be tested. The output of circuit for given test set will be compared by the comparator. The comparator gets the stored response from memory and compare it with the output of CUT. If match occurs for the entire test set then the respective CUT will be considered as PASS otherwise fail. Due to the growth of integrated circuit technology traditional techniques like ATE (Automatic Testing Equipment) are becoming not suitable. Cost of ATE mainly depends on its memory size and its decoder complexity. The need of minimum number of test set is required to reduce the ATE memory and its cost. Minimal test set also reduce the TAT. Accumulator based test pattern generation

exist with LFSR and reseeding concepts for BIST circuit [2, 3]. Those methods are fails to discuss about TAT with minimal test set. Generating new possible test patterns for ISCAS 85 benchmark circuit using arithmetic approach and the response is analyzed in terms of fault coverage and test compaction.

3. PROPOSED SYSTEM

The proposed arithmetic approach is very simple and does not require and complex hardware to generate the test. This approach utilize the existing test set and modify it effectively. It's always wise to improve the test set instead of generating new test set. Mintest vectors are taken as reference and they are modified by using the arithmetic approaches. Hence by doing this, different test patterns will be obtained. The procedure of proposed system is represented in the figure 2. The Mintest vectors of ISCAS 85 has taken. The don't care bits are filled with logic 0 initially. Logic 1 may increase the test power. Then test patterns are reordered in effective way to perform arithmetic approach. Then modulo 2 operation and modulo subtractive operations are performed with successive test patterns. If similar test patterns are exist, they are removed to reduce the test set and the unique test patterns are obtained. The procedure specified as above done using Python 3 programming language. Atalanata 2.0 is used to simulate the new test set for further for obtaining the fault coverage and Test Application time.

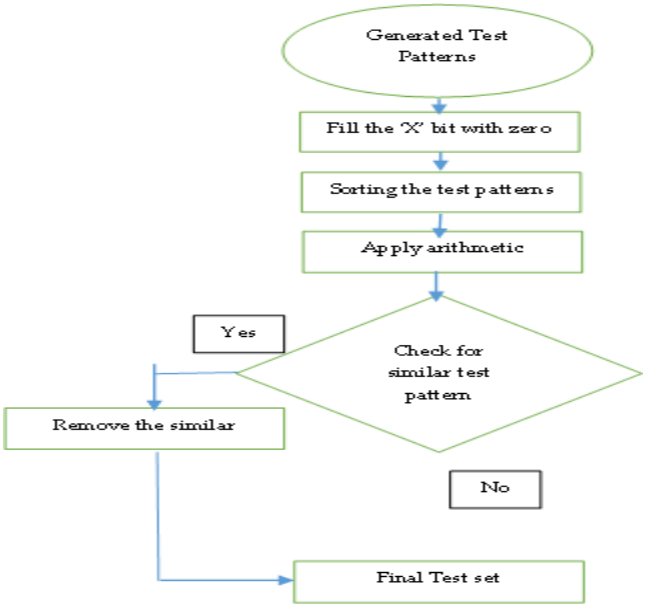

Fig 2. *Proposed Approach*

4. EXPERIMENTAL RESULTS

Test vectors are nothing but the combinations of numbers of 0's and 1's in the obtained final test patterns. XOR and modulo subtraction operation is done and it is observed that only unique test patterns are obtained after those arithmetic approach. Thus, obtaining unique test patterns show that there may be some reduction of test vectors. The reduction of test set from the initial test set is called as Test compaction. The Table 1 shows the analysis of compaction of test vectors after XOR and subtraction operation respectively.

4.1. Test Compaction

The result of test compaction shows that total number of test vectors reduced after the arithmetic operation. For example the circuit C499 have 79 test vectors. It has been found that 24 number of similar test vectors found after the arithmetic approach. Finally the test set for C499 has been reduced to 55.Hence Test compaction is achieved.

Table 1

Results on Test Compaction after the arithmetic approach

ISCAS 85 circuits	Original test vectors	Reduced test vectors (xor)	Reduced test vectors (sub)	Maximum Eliminated Test Count
C499	79	56	55	24
C1355	118	99	99	19
C1908	139	121	121	18
C2670	87	86	86	1
C6288	29	0	28	1

4.2. Test Data Compression:

The Effect of arithmetic approach not only reduce the test vector count also reduces the total test bits. Test data compression is another research area in the field of testing. Several test data compression methods has exists. None of the existing test data compression method describes the reduction of test set. Those methods involves encoding of test data to compress it. They need decoder circuit to decompress the test data. It increase the test complexity. The following Table 2 shows the percentage of test set bits for the arithmetic approach. Figure 3 shows the comparison of modulo 2 arithmetic and modulo subtractive approach respectively.

Table 2

Test Data Compression

ISCAS 85 circuits	Original test bits	Compressed bits (xor)	Compressed bits (sub)	% of compression (xor)	% of compression (sub)
C499	3239	2296	2255	29	30
C1355	4838	4059	4059	16	16
C1908	4587	3993	3993	13	13
C2670	20271	20038	20038	1	1
C6288	928	928	896	0	3

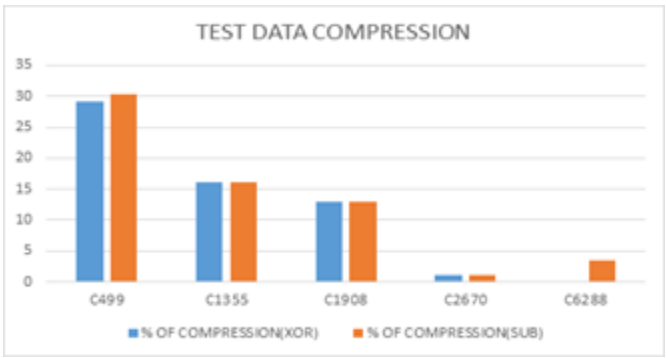

Fig. 3*: Comparison chart of Arithmetic Approach*

4.3. Fault coverage

The reliability of testing is analyzed by Fault coverage and is the ratio of detected faults by total number of faults in the circuit. The result of test compaction is reduction in total test set. Since the total test vectors reduced the quality of testing is need to be measured by means of fault coverage. The fault coverage analysis is described in Table 3 and Table 4. Modulo subtractive approach based test set detects more faults than modulo 2 arithmetic approach.

Fault Coverage = Detected faults/Total number of faults

Table 3
Fault Report Analysis after XOR operation

Circuit name	Total faults	Detected faults	Time consumption	Fault coverage
C499	758	633	0.001	83
C880	942	676	0	71
C1355	1574	1219	0	77
C1908	1879	1537	0	81
C2670	2747	1959	0.016	71
C3540	3428	1737	0.031	50
C5315	5350	4647	0.032	86
C6288	7744	6618	0.015	85

Table 4
Fault Report Analysis after SUB operation

Circuit name	Total faults	Detected faults	Time consumption	Fault coverage
C499	758	656	0.001	86
C880	942	942	0.003	100
C1355	1574	1414	0.008	89
C1908	1879	1713	0.008	91
C2670	2747	2621	0.011	95
C3540	3428	3291	0.002	96
C5315	5350	5291	0.016	98
C6288	7744	7598	0.009	98

4.4 Comparison of arithmetic approach

Atlanta 2.0 is an Automatic Test Pattern Generation and fault simulator tool to detect the stuck-at faults in gate level combinational and sequential circuits [4]. Test Patterns, fault detections and fault report files can be generated using appropriate commands and the fault coverage can be obtained. The ISCAS 85 benchmark circuits are taken and their test patterns are generated and the fault report files for each ISCAS 85 benchmark circuits are obtained by simulating the circuits using Atalanta. Thus, the analysis of report files obtained by Atalanta are shown in the Table 5 and Table 6.

Table 5
Original Mintest Report

ISCAS 85 Circuits	Original Test Set		Reduced Set-Sub		Reduced Set-Xor	
	TAT	FC	TAT	FC	TAT	FC
C499	0.001	93	0.001	86	0.001	83
C880	0.016	100	0.003	100	0	71
C1355	0.004	99	0.008	89	0	77
C1908	0	99	0.008	91	0	81
C2670	0.016	95	0.011	95	0.016	71
C3540	0.016	96	0.002	96	0.031	50
C5315	0.016	98	0.016	98	0.032	86
C6288	0.016	99	0.009	98	0.015	85
AVG	0.011	97	0.007	94	0.012	76

Table 6
Comparative Analysis on Test Application Time

ISCAS 85 Circuits	Original Test Set		Reduced Set-Sub		Reduced Set-Xor	
	TAT	FC	TAT	FC	TAT	FC
C499	0.001	93	0.001	86	0.001	83
C880	0.016	100	0.003	100	0	71
C1355	0.004	99	0.008	89	0	77
C1908	0	99	0.008	91	0	81
C2670	0.016	95	0.011	95	0.016	71
C3540	0.016	96	0.002	96	0.031	50
C5315	0.016	98	0.016	98	0.032	86
C6288	0.016	99	0.009	98	0.015	85
AVG	0.011	97	0.007	94	0.012	76

Table 5 shows the original Mintest report & Table 6 gives comparative analysis on test application time & fault coverage of proposed and original Mintest profile. [5,6]. It's concluded from Table 6 that 31.76% reduction of TAT is obtained for modulo subtractive approach over original test set without more degrading the fault coverage.

5. CONCLUSION

Effective test pattern generation is a major need for current semiconductor industries. Most of the automated tools utilizes the random approach to generate the test set. LFSR is one of the approach, where reseeding of LFSR techniques helps to produce necessary test patterns for CUT. But the complexity of test generator increase with number of inputs. The proposed arithmetic approaches XOR (modulo 2 arithmetic)[5,6] and Subtraction used to modify the test set using python 3 and the TAT, fault coverage for the modified test patterns are analyzed for ISCAS 85 circuits using Atalanta fault simulation tool. The Fault coverage and Test application time are obtained for Subtraction techniques are efficient over modulo 2approach.

6. REFERENCES

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