On Chip Calibration For A 7 Bit Comparator Based Asyncronous Binary Search (CABS) A/D Converter

Vikash Kumar Singh, Kumari Archana

Abstract: An on-chip calibration technique has been proposed for a 7-bit Comparator Based Asynchronous Binary Search (CABS) A/D Converter. The proposed design is veri-fied using an 8-bit, 3.3V, 10 MS/s Asynchronous SAR A/D Converter by integrating the calibration scheme into the A/D Converter. The 8-bit Asynchronous SAR A/D Converter consists of a track-and-hold followed by a two-step conversion process. The two-step architecture consists of a 1-bit course and a 7-bit fine converter. The 1-bit coarse converter is implemented using the SAR-CC principle and the 7-bit fine converter is implemented using the CABS principle. The 7-bit CABS sub-A/D converter consists of 127 comparators with differ-ent threshold voltages. All these 127 comparators with different threshold voltages are calibrated using a calibration technique in which the thresholds are adjusted to the desired value by tuning the total current flowing through the differential pair in the comparator circuit. The calibration technique and the A/D converter have been designed in 0.18 mm CMOS technology with a supply voltage of 3.3 V. The simulation results showed an ENOB of 6.7 for SNDR of 42.09 dB at Nyquist frequency.

Index Terms: 2-step 8-bit ADC Architecture, Calibration of 7-bit CABS ADC, 7-bit CABS stage

1 Introduction

As data conversion interfaces are designed for higher precisions, the non-idealities that accompany monolithic device such as mismatch, non-linearity and finite intrinsic gain of a transistor, limits the raw resolution to approximately 6 bits in CMOS technology. For higher resolutions, it is often necessary to correct for these effects in the design phase itself by means of a circuit or algorithmic techniques. Such techniques are applied to individual building blocks to improve their precision, as well as to the overall architecture to make its output characteristics approach the ideal. In addition to the reg-ular mode of operation, circuits employing some of these techniques typically require a dedicated period to carry out calibration, thereby complicating the system's timing schedule. This project aims at designing an on-chip calibration technique for a 7-bit Comparator Based Asynchronous Binary Search (CABS) A/D Converter. The proposed calibration setup adjusts the threshold voltages to the desired values by tuning the total current flowing through differential pair, thereby reducing the effect of mismatch and process variation. Hence the overall accuracy of the ADC is improved by using cali-bration. The data conversion rate of 10 Mega-Samples Per Second (MS/s) is targeted in this design. Transistor level circuits are designed using 0.18 mm CMOS technology. The circuit design and transient simulations are done in LTspice. The simulation data is exported to MATLAB for frequency domain analysis in order to measure the dynamic performance metrics of the ADC.

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2 Analog to Digital Conversion

Analog to Digital Conversion is an essential function in data processing systems. A/D Converters (ADCs) interface the digital signal processors with the analog world input. This chapter discusses the basic concepts and operations related to A/D conversion followed by the definition of various static and dynamic performance metrics.

2.1 Basic Conversion Principle

Analog-to-digital conversion consists two distinct operations: sampling and quantiza-tion. Sampling converts a continuous time, continuous amplitude analog signal into a discrete time, continuous amplitude signal, while quantization converts the continuous amplitude of this sampled signal into a set of discrete levels. Figure 2.1 shows the principle of A/D conversion.

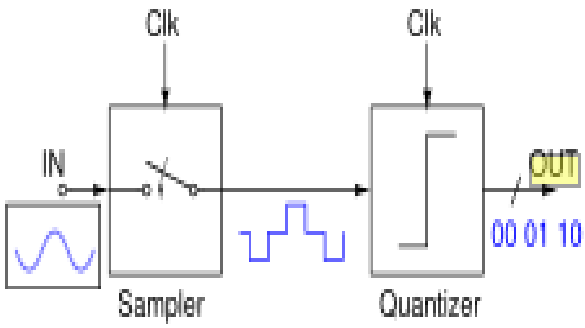


Figure 2.1: Principle of A/D conversion

The I/O characteristics of an ideal 3-bit ADC is shown in Figure 2.2

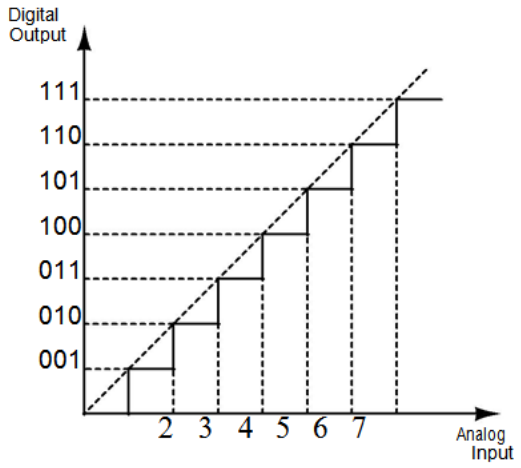


Figure 2.2: Input/output characteristic of 3-bit ADC.

3. 2-step, 8-bit ADC Architecture

3.1 ADC Specifications

The following are the design specifications of the A/D converter.

Supply voltage	3.3 V
Reference voltage	1 V
Architecture	2 step fully differential
Maximum differential input	2 V (peak to peak)
Input common mode	1.65 V
Frequency of operation	10 MS/s
Resolution	8 bits
Technology	0.18 mm CMOS process

3.2 Two step ADC architecture

The 2-step architecture proposed in has been modified for 8-bits and the block dia-gram of 2-step, 8-bit Architecture is shown in Figure 3.1. The 8-bit A/D Converter is implemented using a sample & hold circuit followed by a 2-step conversion pro-cess. The 2-step architecture consists of a 1-bit course and 7-bit fine converter. The 1-bit coarse converter is implemented using the SAR-CC principle and the 7-bit fine converter is implemented using the CABS principle.

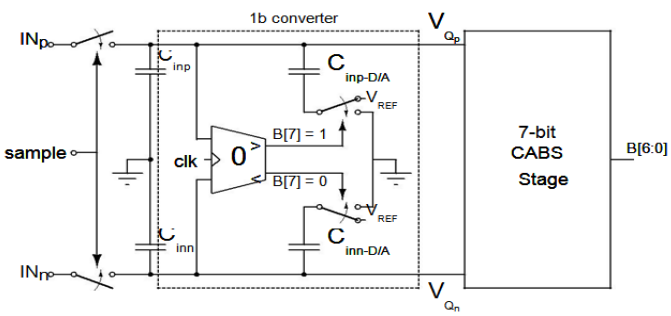


Figure 3.1: 2-step, 8-bit Architecture

Digital output of this 2-step, 8-bit Architecture will be in signed 2's complement form.

- 1-bit SAR gives the sign bit.
- 7-bit CABS stage gives the magnitude bits.

3.2.1 Operation of SAR-CC

The circuit diagram of 1-bit SAR-CC sub A/D converter is shown in Figure 3.2.

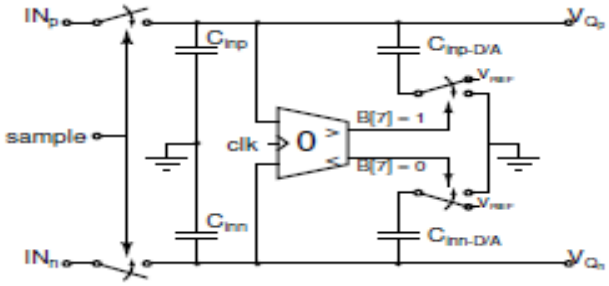


Figure 3.2 SAR-CC sub A/D Convertrer

Initially both the capacitors (i.e, Cinp□D=A & Cinn□D=A) are connected to VREF. Depending on the output of the comparator, one of the capacitor is disconnected from VREF and grounded, in this way subtracting charge on either the positive or negative node. This operation changes both the differential and the common mode signal levels. The operation of SAR-CC can be analyzed mathematically as follows. Let us assume that INp > Inn. Total charge on the node VQp before the comparator makes decision is given by

$$\begin{aligned} Q_1 &= Q_{C_{inp}} + Q_{C_{inp-D/A}} \\ &= V_{IN_p} C_{inp} + (V_{IN_p} - V_{REF}) C_{inp-D/A} \end{aligned} \quad (3.1)$$

Total charge on the node VQp after the comparator makes decision is given by

$$\begin{aligned} Q_2 &= Q_{C_{inp}} + Q_{C_{inp-D/A}} \\ &= V_{Q_p} C_{inp} + V_{Q_p} C_{inp-D/A} \end{aligned} \quad (3.2)$$

By the law of conservation of charges equating Q1 and Q2

$$V_{Q_p} = V_{IN_p} - V_{REF} \left(\frac{C_{inp-D/A}}{C_{inp} + C_{inp-D/A}} \right) \quad (3.3)$$

if Cinpdtoa = Cinp, then eq 3.3 reduces to

$$V_{Q_p} = V_{IN_p} - \frac{V_{REF}}{2} \quad (3.4)$$

Total charge on the node VQn before the comparator makes decision is given by

$$Q_3 = Q_{C_{inn}} + Q_{C_{inn-D/A}}$$
$$= V_{IN_n} C_{inn} + (V_{IN_n} - V_{REF}) C_{inn-D/A} \quad (3.5)$$

Total charge on the node VQn after the comparator makes decision is given b

$$Q_4 = Q_{C_{inn}} + Q_{C_{inn\ D=A}}$$
$$= V_{Q_n} C_{inn} + (V_{Q_n} - V_{REF}) C_{inn\ D=A} \quad (3.6)$$

$$V_{Q_n} = V_{IN_n} \quad (3.7)$$

By the law of conservation of charges equating Q3 and Q4

Similarly for INp < INn, it can be shown that

$$V_{Q_p} = V_{IN_p} \text{ (since no switching of capacitor } C_{inp\ D=A}) \quad (3.8)$$

$$V_{Q_n} = V_{IN_n} - \frac{V_{REF}}{2} \quad (3.9)$$

From equations 3.4, 3.7, 3.8 & 3.9 it is clear that once the 1-bit converter makes a decision, it subtracts a charge which corresponds to VREF2 either from the node VQp or from the node the VQn depending on whether INp > INn or INp < INn. This operation brings the differential signal into the input range of the 7-bit CABS A/D Converter.

3.2.2 Operation of CABS scheme

The operating principle of the CABS converter is based on Asynchronous binary search, the same principle that is used in a successive approximation A/D Converter. But in the CABS architecture instead of approximating the input signal, the comparators with built-in thresholds are used to bracket the input signal. Figure 3.3 shows the CABS architecture instead of approximating the input signal; the comparators with built-in thresholds are used to bracket the input signal. Figure 3.3 shows the CABS architecture illustrated for 3-bits, but it can be extended to more number of bits.

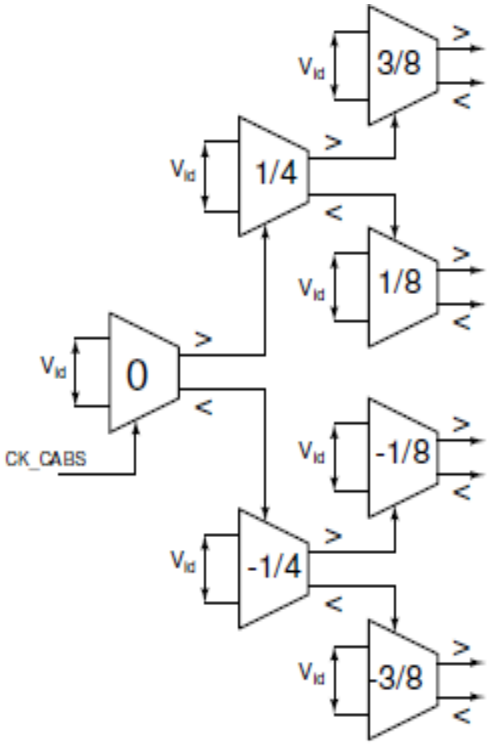


Figure 3.3: CABS A/D converter, shown for 3-bits

Similar to a flash converter, the sampled input signal is applied to all comparators, but all the comparators are not clocked (like in a Flash ADC). Instead the comparators are connected in a binary tree, in which the root comparator compares the input signal with zero and based on its decision synchronously triggers one of the comparator in the next level, (i.e, comparators with threshold 1/4 and -1/4). If the input signal is greater than zero the comparator with threshold 1/4 is triggered, if smaller than zero, the comparator with threshold -1/4 is triggered. This second comparator in turn triggers one of the comparators in the third layer, thereby closing in on the input signal. Based on the outputs of the activated comparators an unsigned binary code is derived: logic 1 is encoded for Input greater than threshold and logic 0 for Input lesser than threshold.

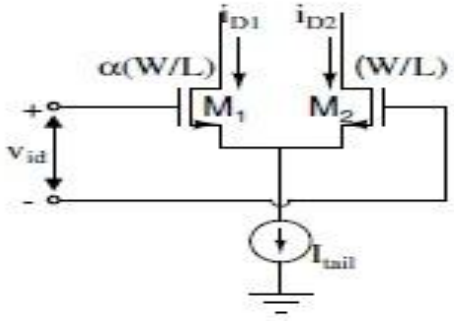
3.2.3 Design of Comparator circuit with embedded threshold

An N-bit CABS stage requires '2N□1' comparators with different built-in threshold voltages. The 3-bit CABS circuit contains 7 comparators each with different built-in threshold voltages. So, the 7-bit CABS stage rquires 127 comparators with different built-in threshold voltages. In order to achieve this it is necessary to know, upon which parameters the comparator threshold depends.

Threshold voltage of an NMOS differential pair

The variation of threshold voltage of an NMOS differential pair is analyzed mathematically as follows.

$$\text{widths } \alpha \left(\frac{W}{L}\right) \text{ and } \left(\frac{W}{L}\right)$$



Fiure 3.4: Differential pair with different (W/L) ratios

From the Figure 3.4 Vid can be written as

$$v_{id} = v_{GS2} - v_{GS1}$$

If M1 and M2 are in saturation, then

$$v_{id} = (V_{th} + V_{DS2,sat}) - (V_{th} + V_{DS1,sat})$$

$$\Rightarrow v_{id} = V_{DS2,sat} - V_{DS1,sat}$$

$$\Rightarrow v_{id} = \sqrt{\frac{2i_{D2}}{k_2}} - \sqrt{\frac{2i_{D1}}{k_1}}$$

$$\Rightarrow v_{id} = \sqrt{\frac{2i_{D2}}{\alpha k}} - \sqrt{\frac{2i_{D1}}{k}} \qquad (3.10)$$

$$\text{And we have} \quad I_{tail} = i_{D1} + i_{D2} \qquad (3.11)$$

Solving the equations 3.10 & 3.11 for iD1 & iD2, we get

Now we can obtain the threshold by finding vid at which iD1-iD2 = 0. Therefore by solving iD1□iD2 = 0 for Vid, we get

$$\text{Threshold Voltage } v_{id} = \sqrt{\frac{I_{tail}}{k}\left\{\left(\frac{\alpha+1}{\alpha}\right) - \frac{2}{\sqrt{\alpha}}\right\}} \qquad (3.14)$$

The variation of threshold voltage for different values of 'a' is shown in Figure 3.5. From the equation 3.14, it is clear that the threshold voltage can be controlled by I tail and a (i.e, ratio ofW/L)s of M1 and M2 transistors of NMOS differential pair shown in Figure 3.4). So, comparator circuits with different threshold voltages are designed using a differential pair by properly choosing Itail and values.

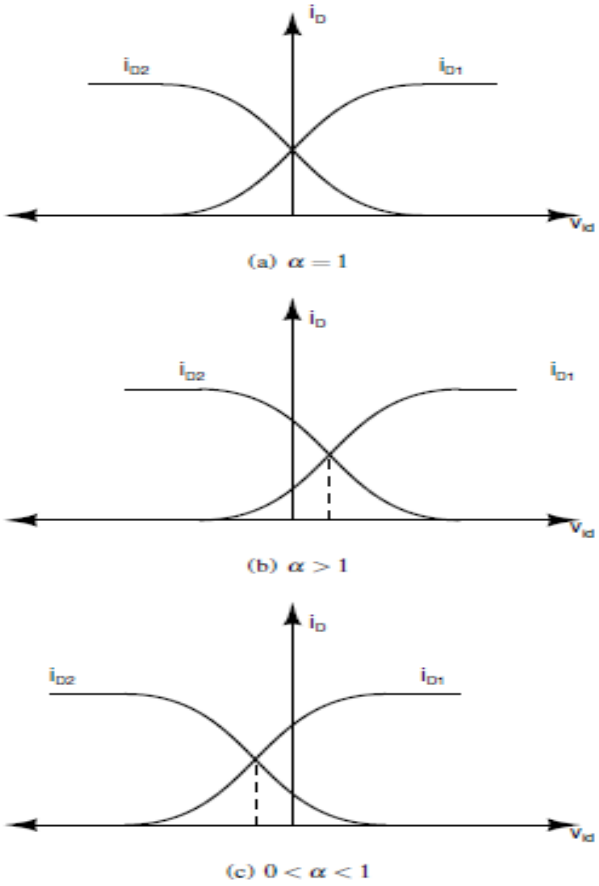


Figure 3.5: Threshold variation of a comparator

Comparator circuit and its operation

Basically a comparator consists of three components. They are

- Current mirroring circuit (M3 through M6)
- PMOS differential pair (M1 and M2)
- latch circuit (M7 through M10)

This comparator circuit operates in two phases. They are

- Reset Phase (i.e, when Comp signal is at logic '0'): In this phase, all the internal nodes of latch are grounded by using M11 through M14 transistors and the mirroring circuit is turned OFF by using M4 and M6. In this phase, both the outputs (Greater & Lesser) will be at logic '0'.

- Comparison Phase (i.e, when Comp signal is at logic '1'): In this phase, the applied differential input to the differential pair is compared with the threshold voltage and based on the comparison, one of the output's of the comparator goes to logic '1' and the other goes to logic '0' i.e, if the differential input is greater than the threshold voltage of the comparator then 'Greater' signal becomes logic'1' and 'Lesser' signal becomes logic'0'and vice-versa.

Specifications of some of the comparators are shown in the Table 3.1.

Table 3.1: Specifications of the Comparators

Comparator Threshold(V)	Clock Delay Required(ns)	Decision Time(ns)	No. of fingers of size ($0.25\mu/0.18\mu$)i.e(2n)	Size of M_1	Current (μA)
63/128	4	1	702	$2\left(\frac{8\mu}{0.36\mu}\right)$	150
55/128	4	1	574	$2\left(\frac{8\mu}{0.36\mu}\right)$	150
45/128	3	1.2	426	$2\left(\frac{6\mu}{0.36\mu}\right)$	150
37/128	3	1.6	312	$2\left(\frac{6\mu}{0.36\mu}\right)$	150
30/128	3	1.8	248	$2\left(\frac{4\mu}{0.36\mu}\right)$	100
26/128	3	2.3	196	$2\left(\frac{4\mu}{0.36\mu}\right)$	100
22/128	3	3	148	$2\left(\frac{4\mu}{0.36\mu}\right)$	100
19/128	3	2	230	$2\left(\frac{2\mu}{0.36\mu}\right)$	100
11/128	3	2.5	190	$2\left(\frac{1.5\mu}{0.36\mu}\right)$	100
8/128	3	4	108	$2\left(\frac{1.5\mu}{0.36\mu}\right)$	100
7/128	3	2.8	168	$2\left(\frac{1.3\mu}{0.36\mu}\right)$	100
4/128	3	3.6	114	$2\left(\frac{1.2\mu}{0.36\mu}\right)$	100
3/128	3	2	208	$2\left(\frac{1.1\mu}{0.36\mu}\right)$	100
2/128	3	3.2	146	$2\left(\frac{1.08\mu}{0.36\mu}\right)$	100
1/128	3	3.2	142	$2\left(\frac{1.04\mu}{0.36\mu}\right)$	100

4. CALIBRATION OF 7-BIT CABS ADC

4.1 NEED FOR CALIBRATION

Once the ADC is fabricated, due to process variations, there will be transistor mismatches. So, the transistor mismatches introduce non-linearity in the current mirroring circuit. Because of the transistor mismatches and the non-linearity in the current mirroring circuit, the threshold voltage of the comparator deviates from the desired value. Hence, non-linearity is introduced in the overall ADC design. So, it is necessary to calibrate the comparators so that the effect of process variation is minimized.

4.2 CALIBRATION OF AN INDIVIDUAL COMPARATOR

Threshold voltage for an NMOS differential pair having widths is proportional to (W/L) and (W/L) asshown in Figure 4.1 is given by

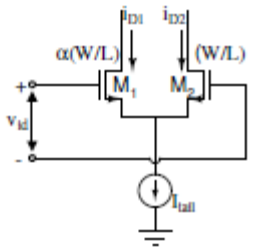


Figure 4.1: Differential pair

So, it is clear that the threshold voltage of a comparator can be adjusted by varying the 'Itail' and/or 'a' (i.e, the ratio of (W/L)s of the differential pair). So, in this project calibration is done by tuning the tail current. In the proposed calibration scheme 'Itotal' is implemented as shown in Figure 4.2. During the calibration mode, the desired value of threshold has to be applied as input to the corresponding comparator. A 5-bit counter is used to tune the current to the desired value. The output of the counter is connected to binary weighted current sources having an LSB of 1mA. Since a 5-bit counter is used, the available range for tuning is 32mA with a step size of 1mA.

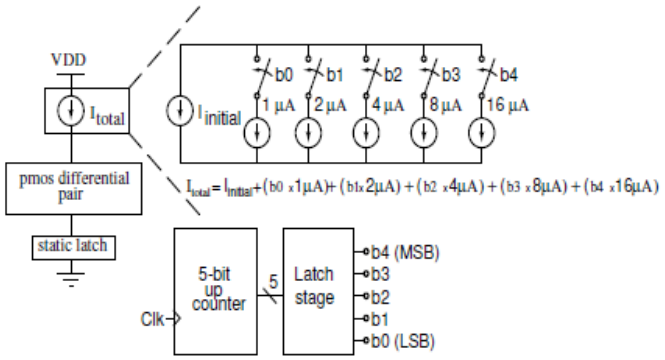


Figure 4.2: Implementation of 'Itotal'

4.2.1 CALIBRATION SETUP FOR A POSITIVE THRESHOLD VOLTAGE COMPARATOR

For a positive threshold voltage comparator, 'Iinitial' is set such that

$$I_{initial} = I_{total}(\text{i.e, desired value}) + 16\,\mu A \qquad (4.1)$$

Here the 5-bit counter acts a down counter. So, the initial value of the counter is all 1's, which means all the binary eighted current sources are turned ON thereby setting 'Itotal' greater than the desired one. This implies that the threshold has been set to a value greater than the desired value. So the 'Lesser' and 'Greater' output's of the comparator will be logic 'high' and logic 'low' respectively. The counter is decremented by one for every clock cycle and based on the counter code a finite even number of fingers (each pair of fingers carrying a current of 1mA) gets turned ON. Initially Itotal has been set to a value greater than the desired value. For every clock cycle Itotal is decremented by 1mA. After some clock cycles, when the 'Itotal' reaches the desired value, the output flips i.e, 'Greater' becomes logic 'high' and 'Lesser' becomes logic 'low', then the latch gets disabled thereby holding the counter code for which the outputs have flipped and thus completing the calibration process. Figure 4.3 shows the circuit diagram of the comparator circuit having positive threshold voltage with the calibration setup included. Here the comparator has two modes of operation i.e, calibration mode and normal mode. In the calibration mode (i.e, when 'calib' signal becomes logic '1'),

- Desired threshold voltage is applied across the PMOS differential pair and it is held till the calibration of the comparator is complete.
- Depending on the counter code a finite number of fingers is turned ON.
- For each clock cycle, the comparator compares the applied differential input (Desired threshold voltage) with the present threshold voltage i.e, set by turning

on a finite number of fingers in the current mirroring circuit. The comparator makes a

- decision based on the comparison for every clock cycle.
- Once the desired threshold is set, the latch gets disabled and the counter value is held and thus fixing the number of fingers to be connected in the current mirroring circuit. This completes the calibration phase for that comparator.
- Since the initial state of latches is not known, latch output nodes are groundedusing M30 through M34 transistors.
- M25 through M29 transistors are used to turn ON all the fingers initially.

In the normal mode (i.e, when 'calib' signal becomes logic '0'),

• For each clock cycle, the comparator compares the differential input signal applied across the PMOS differential pair with the it's threshold voltage. The comparator makes a decision based on the comparison for every clock cycle.

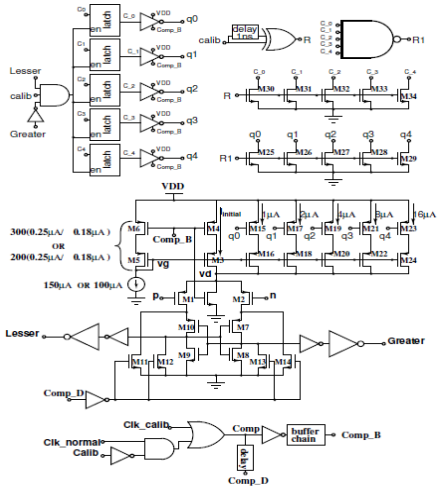


Figure 4.3: Circuit diagram of a positive threshold voltage comparator

4.2.2 CALIBRATION SETUP FOR A NEGATIVE THRESHOLD VOLTAGE COMPARATOR

For a negative threshold voltage comparator 'Iinitial' is set such that

Here the 5-bit counter acts a up counter. So, the initial value of the counter is all 0's, which means all the binary weighted current sources are turned OFF thereby setting 'Itotal' lesser than the desired one. This implies that the threshold has been set to a value lesser than the desired value. So the 'Lesser' and 'Greater' output's of the comparator will be logic 'low' and logic 'high' respectively. The counter is incremented by one for every clock cycle and based on the counter code a finite even number of fingers (each pair of fingers carrying a current of 1mA) gets turned ON. Initially Itotal has been set to a value lesser than the desired value. For every clock cycle Itotal is incremented by 1mA. After some clock cycles, when the 'Itotal' reaches the desired value, the output flips i.e, 'Greater' becomes logic 'low' and 'Lesser' becomes logic 'high', then the latch gets disabled thereby holding the counter code for which the outputs have flipped and thus completing the calibration process. In the calibration mode (i.e, when 'calib' signal becomes logic '1'),

$$I_{initial} = I_{total}(\text{i.e, desired value}) - 16\,\mu A \qquad (4.2)$$

- Desired threshold voltage is applied across the PMOS differential pair and it is held till the calibration of the comparator is complete.
- Depending on the counter code a finite number of fingers is turned ON.
- For each clock cycle, the comparator compares the applied differential input (Desired threshold voltage) with the present threshold voltage i.e, set by turning on a finite number of fingers in the current mirroring circuit. The comparator makes a
- decision based on the comparison for every clock cycle.
- Once the desired threshold is set, the latch gets disabled and the counter value is held and thus fixing the number of fingers to be connected in the current mirroring circuit. This completes the calibration phase for that comparator.
- Since the initial state of latches is not known, latch output nodes are grounded using M25 through M29 transistors.

In the normal mode (i.e, when 'calib' signal becomes logic '0'),

- For each clock cycle, the comparator compares the differential input signal applied across the PMOS differential pair with the it's threshold voltage. The comparator makes a decision based on the comparison for every clock cycle.

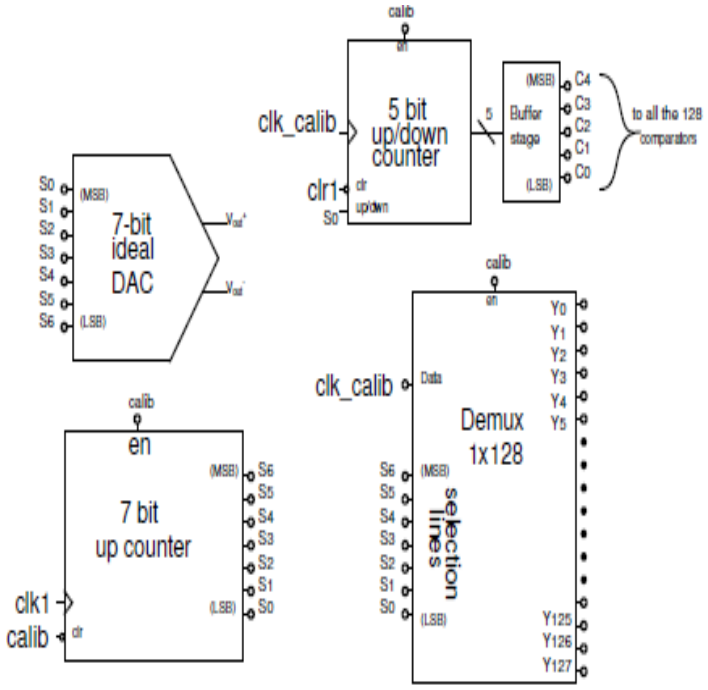
4.3 CALIBRATION SETUP FOR THE 7-BIT CABS A/D CONVERTER

This calibration scheme employs only one 5-bit up/down counter to calibrate all the 127 comparators of the CABS. So, only one comparator can be calibrated at a time. This project requires calibration of 127 comparators one after the other. So to select one comparator out of 127 comparators for calibration, a 1x128 Demux is used. Here, the comparators are calibrated in a particular order (i.e, level by level starting from MSB to LSB) so that an error in one level due to threshold variation, is not carried to the next level.

Figure 4.4 shows the calibration setup required for calibrating all the 127 comparators.

Figure 4.4: Calibration set up for the entire ADC

The output pins of the Demux should be connected to comparators in such a way that they are calibrated level by level. A 7-bit up-counter is used to generate selection lines for Demux and the same counter codes are applied as input to ideal 7-bit DAC, so as to generate the required input threshold voltages during calibration. Since a 5-bit up/down counter is used for calibration, a maximum of 32 clock cycles are required for calibrating each comparator. DAC generates a differential Analog voltage corresponding to that code and is applied to all the comparators. At the same time 1x128 Demux selects one of the 127 comparators for calibration and the Clock signal is applied to that comparator only. Based on the LSB of 7-bit up counter, the operation of 5-bit counter (i.e, whether it should act as up/down counter) is decided. 5-bit counter increments/decrements for each clock cycle. After 32 clock cycles, the 7-bit up counter code is incremented by 1 and the 5-bit counter is cleared. Now the new 7-bit up counter code is applied as input to ideal DAC and 1x128 Demux and the process continues until all the comparators are calibrated. The flowchart for the calibration process is shown in the Figure 4.5



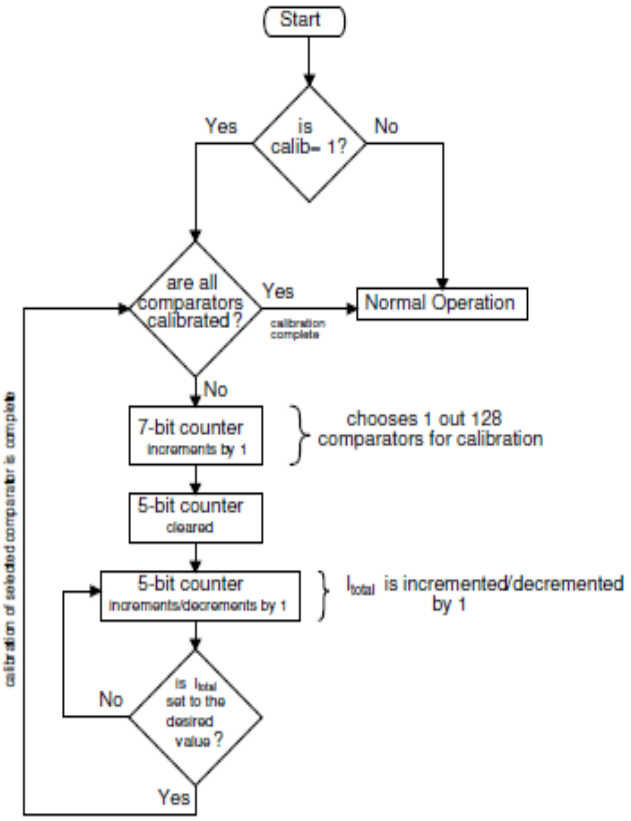


Figure 4.5: flowchart for the calibration process

Clock signal for 7-bit up counter and clear signal for 5-bit up/down counter has been generated as shown in Figure 4.9. The reference threshold voltages required generated by DAC during calibration has to be applied from the front end of the ADC i.e, it has to be applied to the 1-bit SAR stage. But the 1-bit SAR subtracts Vref 2 from the applied input. To avoid this, the first stage (1-bit SAR) has to be by-passed during calibration phase. This is achieved by adding some additional circuit as shown in the Figure 4.6 with dotted lines.

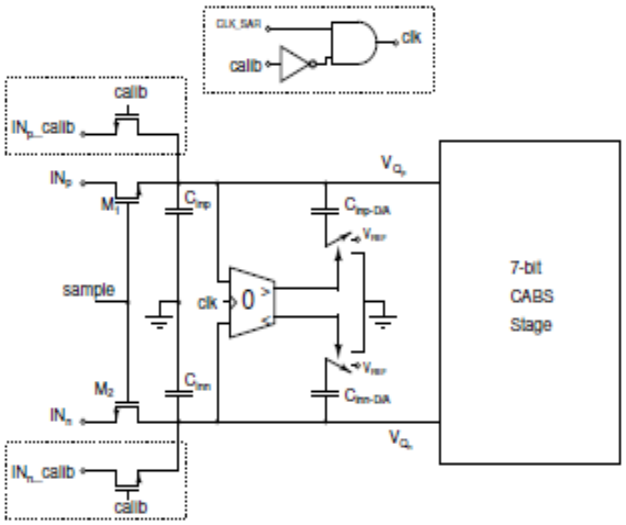


Figure 4.6: 1-bit SAR

5. RESULTS

5.1 TIME-DOMAIN ANALYSIS

5.1.1 CALIBRATION PHASE

The designed ADC is operated in calibration phase (i.e, by setting 'calib' signal to logic '1'). The calibration phase of comparators with threshold voltages (32/128)V and -(32/128)V are shown in Figure 5.1 & 5.2. As mentioned earlier, the desired threshold voltage is applied as input to the comparator in the calibration phase. The desired threshold voltages has been generated using an ideal DAC and applied to the comparator during calibration phase.

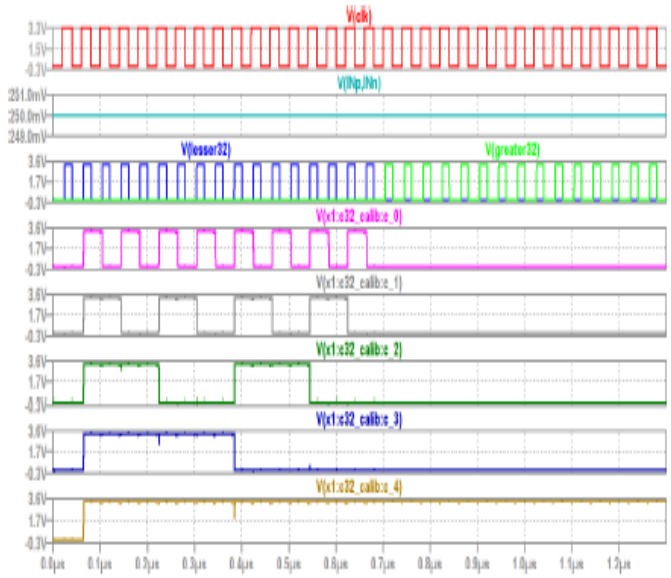


Figure 5.1: Calibration phase of (32/128) V threshold voltage Comparator

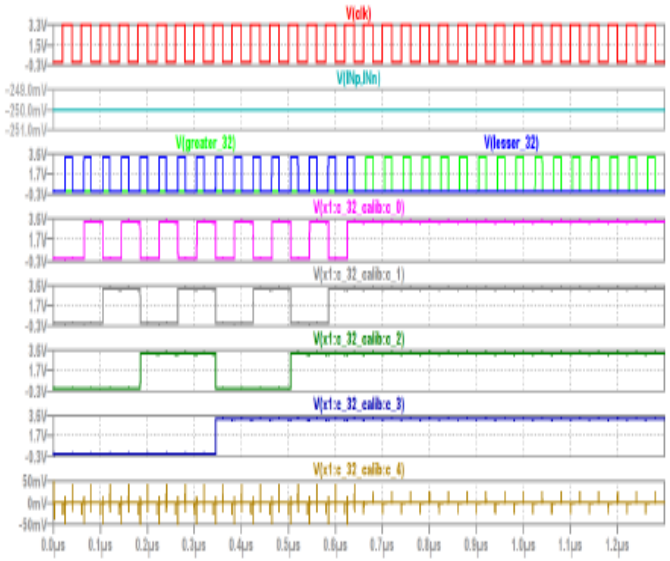


Figure 5.2: Calibration phase of -(32/128) V threshold voltage Comparator

Figure 5.3 shows the calibration phases of comparators with threshold voltages (32/128)v, -(32/128)v, (16/128)v, -(48/128)v and (48/128)v. here calibration is performed level by level. (32/128)v and -(32/128)v threshold voltage comparators belong to first level and the remaining belong to second level.

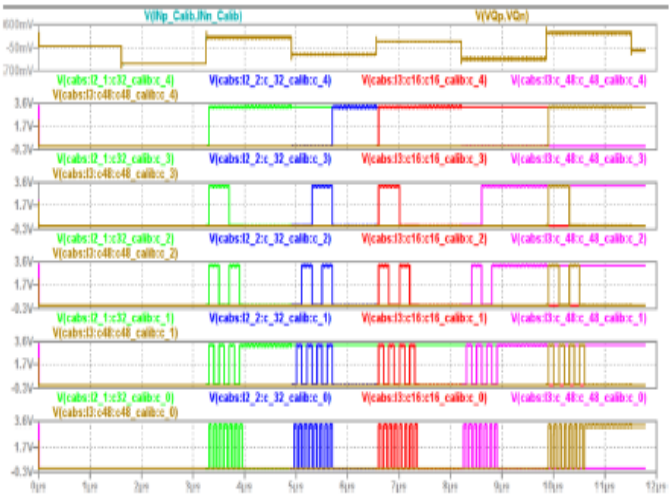


Figure 5.3: Calibration phases of 1st and 2nd level Comparators

5.1.2 7-BIT CABS STAGE

The 7-bit CABS ADC is applied with a differential inputs of (61/128)V, (62/128)V and (63/128)V respectively with a DC common mode voltage of 1.4V as shown in the Table 5.1. A clock signal of 10MHz frequency, having a duty cycle of 50% is used foroperating the ADC.

Table 5.1: Inputs applied to 7-bit ADC at different time instants

Simulation Time (ns)	Applied Input (V)	Desired Output Code
0 ns to 100 ns	$\left(\frac{61}{128}\right)$	1111101
100 ns to 200 ns	$\left(\frac{62}{128}\right)$	1111110
200 ns to 300 ns	$\left(\frac{63}{128}\right)$	1111111

Figure 5.4 shows the simulation result of the 7-bit CABS ADC for the above input conditions. Here 'b6' corresponds to MSB and 'b0' corresponds to LSB. CABS stage was observed with all the possible combination of inputs and the worst case time taken by the CABS stage for producing the digital code is 38 ns.

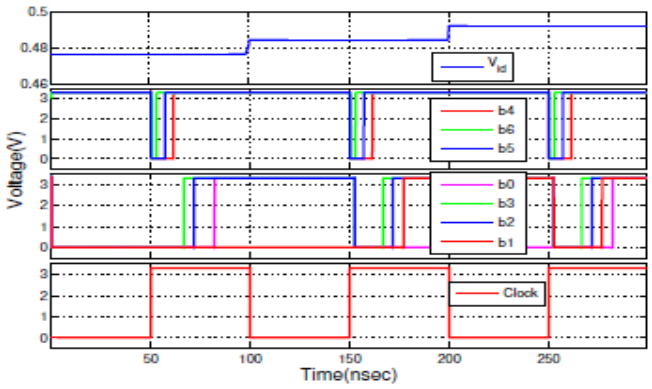


Figure 5.4: Simulation result of CABS stage

5.2 Frequency-Domain Analysis

5.2.1 The complete ADC System

A 100 KHz sinusoidal input of amplitude 1.0 V and DC level 1.65V (amplitude varies between 0.65 to 2.65 V) is applied to the designed 2-step, 8-bit ADC and the digital code generated by ADC is applied to an ideal DAC (Spice code taken from) and the simulation data is exported to MATLAB. Figure 5.5 shows the input of an ADC and the output of DAC with both DC levels adjusted to 0V and Figure 5.6 shows the power spectrum of input of an ADC and the output of DAC.

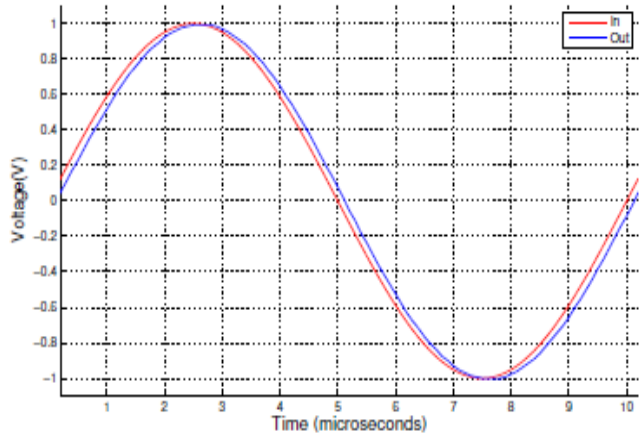


Figure 5.5: Response of 8-bit ADC for Sinusoidal input of 100 KHz

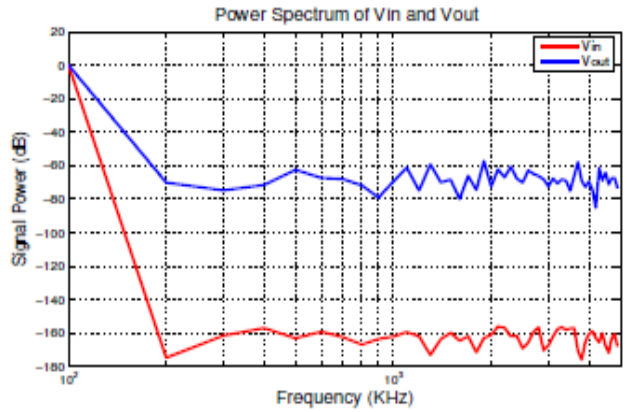


Figure 5.6: Power Spectrum of 8-bit ADC for Sinusoidal input of 100 KHz

5.3 Performance Metrics

The performance specifications are measured from multiple transient simulations and the calculated average values are listed in the Table 5.2. The offset error and gain error shown in the table are normalized w.r.t LSB.

Table 5.2: Measured performance parameters of SAR ADC

Parameter	Measured Value
Offset Error	0.083
Gain Error	0.065
Latency	One clock cycle
SNDR @ Nyquist frequency	42.08 dB
SNDR @ 2.5 MHz	42.08 dB
SNDR @ 100 KHz	48.72 dB
Power	145 mW/ Conversion step
Overall calibration time for the 7-bit ADC	4224 clock cycles

6 CONCLUSION

An on-chip calibration technique has been designed for a 7-bit Comparator based Asynchronous Binary Search (CABS) ADC. The on-chip calibration has been verified by using the 7-bit CABS ADC as a second stage in an 8-bit, 10 MS/s Asynchronous SAR ADC. The calibration phases of each comparator in the 7-bit ADC have been thoroughly verified. The 7-bit CABS ADC takes 4224 clock cycles for the entire calibration process In the proposed calibration technique, each comparator is alloted a fixed amount of time (33 clock cycles) for calibration. This can be reduced by selecting the next comparator (which is to be calibrated) once the desired threshold voltage is set for the comparator (which is being calibrated). The overall calibration time for the 7-bit ADC can also be reduced by using a higher frequency (twice) clock signal, for calibration. However the overall ruggedness of the calibration technique can only be verified after fabricating the IC.

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