Design and Reliability Analysis of Reliable Irregular Shuffle Exchange Network (RISEN)

Shobha Arya, Nipur Singh

Abstract — The performance of multiprocessor systems, parallel and distributed systems depends on its interconnection networks. The Multistage Interconnection Network (MIN) is an interconnection network in which predefined topology has several layers of systematic interlinked switching elements (SE) that allow processors and memory modules to communicate with each other. This paper examines the reliability of the proposed network named as Reliable Irregular Shuffle Exchange Network (RISEN) and compares it with the existing Irregular Augmented Shuffle Exchange Network-4 (IASEN-4). Routing algorithm shows that RISEN is a multipath Multistage Interconnection Network (MIN) which can withstand faults and provides alternate paths between a source-destination pair with dynamic rerouting ability. The performance and comparison analysis exhibit that the proposed RISEN is more reliable and fault tolerant as compared to the existing MIN.

Index Terms — Multistage Interconnection Network, Fault tolerance, Reliability, Switching elements

1 INTRODUCTION

Reliability, fault tolerance, and cost-effectiveness are the dominant issues in Multistage Interconnection Networks (MINs) performance. The reliability of MIN can be increased by handling more faults in various switching stages. MINs are faster, low-cost networks and they are used in Single Instruction Multiple Data (SIMD) and Multiple Instruction Multiple Data (MIMD) computers. Based on topologies the MINs can be classified as follows: Regular, Irregular, and Hybrid. The regular MIN consists of the same number of switching elements (SE) in each stage [15]. In irregular MIN, the number of switching elements (SE) is not the same in each stage [15]. The hybrid MIN consists of the properties of regular MIN as well as the properties of irregular MIN also [15]. The performance of MIN can be measured in terms of fault tolerance, reliability and permutation capability. The reliability can be classified into two types such as hardware reliability [12] and software reliability [11] [15]. The hardware reliability can be defined on the basis of time but software reliability cannot [11]. In hardware reliability, how much time the hardware remain functioning without any fault. In this paper, the focus is given to the hardware reliability of the MINs. Simple series-parallel probabilistic combinations, upper bound & lower bound of Mean Time to Failure (MTTF) are used to compute reliability [15]. MTTF of RISEN is measured through the criterion of “full access” and “switch fault or dead-fault” model. The full access criterion implies the ability to reach from any input to any output precisely in one pass even some switching components or segments (crossbar switches, MUX, DEMUX) may be defective or faulty but not the whole network [13][15] and this failure of segments doesn’t influence the reliability of others for example switch failure occurs individually. In switch-fault or dead fault model, failure or fault in a switch makes it totally ineffective and non-working [13][15]. MTTF is the expected time elapsed before some source is disconnected from some destination [13][14][15].

A limited work has been done on the reliability of irregular MINs [8],[9],[10],[13]. In this paper, we are focusing on existing irregular MIN named as Irregular Augmented Shuffle Exchange Network-4 (IASEN-4) [14] and create a modified MIN named as Reliable Irregular Shuffle Exchange Network (RISEN). The main drawback of IASEN-4 is less reliability and having less alternate paths between any source-destination pair with less accessibility [1] in non-faulty (when there is no faulty node in each stage) and faulty (when a faulty node exists in one or more stages) cases. Therefore, a new MIN named as Reliable Irregular Shuffle Exchange Network (RISEN) has been proposed to resolve this issue. RISEN is more reliable and it provides more alternate paths in faulty and non-faulty cases. This paper addresses the issue of reliability and improves the performance of the proposed network by reducing the count of links in the proposed RISEN.

We compared the reliability of proposed RISEN with existing Irregular Augmented Shuffle Exchange Network-4 (IASEN-4). In section 2, the structure of existing MIN (IASEN-4) and proposed MIN (RISEN) has been described. The generalized link connection formula is also given for RISEN in each stage. Section 3 describes the routing scheme of RISEN in which redundancy graph and routing algorithm is given. Section 4 describes the reliability analysis of existing and proposed MINs. Section 5 concentrates on the cost-effectiveness of both MINs. At last conclusion has been described in section 6.

2 STRUCTURE AND DESIGN OF MINS

The structure of the existing IASEN-4 and proposed RISEN are discussed below

2.1 Irregular Augmented Shuffle Exchange Network-4 (IASEN-4)

IASEN-4 is an N×N network which consists of N sources, N destinations, N Multiplexers (MUX) and N Demultiplexers (DEMUX) with \((\log_2 N)\) stages [14]. The first and last stage consists of \(2 \times 2\) switching elements (SE) whereas intermediate stages consist of the \(2^{15}\) number of switching elements (SE), where \(n = \log_2 N\). The size of MUX and DEMUX is \(4\times1\) and \(1\times4\) respectively. The first stage, intermediate stage, and last stage have SEs of size \(2\times3\), \(4\times2\), and \(2\times2\) respectively. SEs of each stage is associated with each other through alternative links [14].

2.2 Reliable Irregular Shuffle Exchange Network (RISEN)

The Reliable Irregular Shuffle Exchange Network (RISEN) has N sources and N destinations, which are connected, with N multiplexers (MUX) and N demultiplexers (DEMUX) respectively. The size of each MUX and DEMUX in RISEN is \(4\times1\) and \(1\times4\) respectively. RISEN has \(n\) number of stages, range from 0 to \((n-1)\), where \(n = \log_2 N\). Stage 0 and last stage consist of \((N/2)\) number of switching elements (SE). There are \((n-2)\) middle stages \((m)\) in the network. Each middle stage \((m)\) consists of \(N/4\) number of SEs. In stage 0, each SE is attached with two MUX of size \(4\times1\) and in the last stage; two DEMUX of size \(1\times4\) are connected with each SE. The SEs of
RISEN consists of two identical sub-networks, which are denoted by \(G^a\) where \(a=0\) or \(1\), based on the most significant bit (MSB) of the destination address. If MSB is 0, then half of the source-destination terminals falls into the \(G^0\) and the others having MSB 1 fall into \(G^1\). For example, in Fig. 1, SE \(0_0, 1_0, 2_0, 3_0\) belonging to stage 0 of a subnetwork \(G^0\) form a conjugate subset, switches \(0_0\) and \(2_0\) form one conjugate pair, and switches \(1_0\) and \(3_0\) form another conjugate pair. Each subnetwork is associated with all sources and all destinations with the help of MUX and DEMUX respectively. The SEs of each stage is connected with SEs of the next stage through links. The link connection pattern from source to destination is as follows:

(1) Link Connections at Source:
Each source is connected with four multiplexers (MUX) as follows:

(i) For each source \(S_i\), where \(i=0\) to \((N/4)-1\)
(a) First link connects to MUX \((i)\)
(b) Second link connects to MUX \((i+(N/4))\)
(c) Third link connects to MUX \((i+(N/2))\)
(d) Fourth link connects to MUX \((i-(N/4))\)

(ii) For each source \(S_i\), where \(i=(N/4)\) to \((N-1)\)
(a) First link connects to MUX \((i)\)
(b) Second link connects to MUX \((i-(3N/4))\)
(c) Third link connects to MUX \((i-(N/2))\)
(d) Fourth link connects to MUX \((i-(N/4))\)

(2) Link Connections at MUX:
The RISEN consists of \(N\) number of multiplexers (MUX) with size \(4\times1\), range from 0 to \((N-1)\). Each switch \(j_0\), where \(j=0\) to \(N/2-1\), in stage 0 is connected with two MUX with following steps:

(a) First link connects to MUX \((2j)\)
(b) Second link connects to MUX \((2j+1)\)

(3) Link Connections at stage 0:
Each SE in the middle stage is connected with four SEs of stage 0. We assume that the total number SE in stage 0 is divided into \(N/8\) groups \((P_q)\), where \(q=0\) to \(N/8-1\). Each the group \((P_q)\) consists of four SEs. Each SE of group \((P_q)\) has 3 output links. Each SE \(j_0\) of stage 0 is connected with 3 output links:

(a) First link connects to SE \((j_{n-1})\) of last stage
(b) Second output link connects to SE \((2q)_1\) of stage 1
(c) Third output link connects to SE \((2q+1)_1\) of stage 1

(4) Link Connections from stage 1 to stage (n-3):
In this step, stages \(m=1\) to \((n-3)\) are considered except the last middle stage. Each stage consists of \(N/4\) number of SEs. There are \(N/8\) groups \((P_r)\) in each stage, where \(r=0\) to \((N/8)-1\). Each group consists of two switching elements (SEs). Each SE of each group \((P_r)\) has two output links. These output connection links are as follows:

(i) The SE \((k=2r)_m\) of stage m has 2 output links:
(a) First link connects to SE \((2r)_m\) of next stage
(b) Second link connects to SE \((2r+1)_m\) of next stage

(ii) The SE \((k=2r+1)_m\) of stage m has 2 output links:
(a) First link connects to SE \((2r+1)_m\) of next stage
(b) Second link connects to SE \((2r+1)_m\) of next stage

(5) Link Connections from stage (n-2):
In this case, when network size is \(N=16\). There are \(N/4\) switching elements (SE) in stage 2. Each switching element (SE) has two output links. There are two cases to determine the link connections of SE: (i) When SE is Even and (ii) When SE is Odd. A SE \(k_2\) at stage 2 is even SE if \(k\)mod2=0, otherwise it is an odd SE.

(i) When SE \(k_{n-2}\) of stage \((n-2)\) is even then the output link connections are as follows:
(a) First link connects to SE \((2k+2)_{(n-1)}\) of last stage
(b) Second link connects to SE \((2k+3)_{(n-1)}\) of last stage

(ii) When SE \(k_{n-2}\) of stage \((n-2)\) is odd then the output link connections are as follows:
(a) First link connects to SE \((2k-2)_{(n-1)}\) of last stage
(b) Second link connects to SE \((2k-1)_{(n-1)}\) of last stage

(6) Link Connections at last stage (n-1):
The last stage \((n-1)\) consists of \(N/2\) number of SEs. Each SE \(j_{n-1}\) has 2 output links, where the range of \(j=0\) to \((N/2-1)\). Therefore, the output link connections of each SE \(j_{n-1}\) of the last stage are as follows:

(a) First link connects to DEMUX \((2)\)
(7) **Link Connections at DEMUX:**
The link connections at DEMUX consist of following steps:

(i) Each destination D_i is connected with four DEMUX, where i=0 to ((N/4)-1)
   (a) First link connects to DEMUX (i),
   (b) Second link connects to DEMUX (i+(N/4))
   (c) Third link connects to DEMUX(i+(N/2))
   (d) Fourth link connects to DEMUX (i+(3N/4))

(ii) Each destination D_i is connected with four DEMUX, where i=(N/4) to ((N/2)-1)
    (a) First link connects to DEMUX (i)
    (b) Second link connects to DEMUX (i+(N/4))
    (c) Third link connects to DEMUX(i+(N/2))
    (d) Fourth link connects to DEMUX (i+(3N/4))

(iii) Each destination D_i is connected with four DEMUX, where i=(N/2) to ((3N/4)-1)
     (a) First link connects to DEMUX (i)
     (b) Second link connects to DEMUX (i+(N/4))
     (c) Third link connects to DEMUX(i+(N/2))
     (d) Fourth link connects to DEMUX (i+(3N/4))

(iv) Each destination D_i is connected with four DEMUX, where i=(3N/4) to (N-1)
     (a) First link connects to DEMUX (i)
     (b) Second link connects to DEMUX (i-(3N/4))
     (c) Third link connects to DEMUX (i-(N/2))
     (d) Fourth link connects to DEMUX (i-(N/4))

3 **Routing Scheme of RISEN**

3.1 Redundancy Graph
The redundancy graph describes the all possible path between a source and destination address. The arrow symbol shows the alternate direct connections in the network to bypass the request in a similar stage if the switch in its next stage is busy or faulty. The RISEN network is not only cost-effective in comparison to existing IASEN-4 Networks but the performance measure in terms of the number of paths is also better. The redundancy graph representation of RISEN is shown in Fig. 2.

![Fig. 2 Reliable Irregular Shuffle Exchange Network (RISEN)](image)

3.2 Routing Algorithm
Routing procedure for a RISEN describes how a request from any source travels through the different intermediate stages and reaches to a given destination. The RISEN is the self-routing network. It is assumed that each source-destination pair tries to use only one path at a time. It is considered that the source & switches have the capacity to detect faults in the switches to which they are connected. In RISEN, each source is associated with two switches in a subnetwork.

The idea of dynamic re-routing has been utilized to locate a substitute path from the present stage in case of a fault. In other words, if a fault occurs in any stage, a switching element (SE) in the previous stage will re-route data or message through an alternative path or link.

Let S_1 and D_i are the source and destination addresses respectively. Let binary representation of the source S_i and destination D_i is as follows:

S_i=s_0, s_1, ..., s_n, s_n+1, D_i=d_0, d_1, ..., d_n, d_n+1, where i=0 to N-1

A source S_i selects a particular subnetwork (G^0) based upon the most significant bit (MSB) of the destination address and attempts entry into the RISEN via its primary path. If the primary path is faulty (i.e. MUX or switch or both are faulty), the request is routed through the secondary path. For example, for source 0, SE (0_0) is the primary SE (PSE_0) and (2_0) is first alternate SE (FSE_0) in stage 0 in subnetwork G^0 through its primary and secondary path respectively. SE 4_0 and 6_0 are second alternate SE (SSE_0) and third alternate SE (TSE_0) for subnetwork G^1 in stage 0 through its primary and secondary path respectively. The first step of the routing of RISEN is to obtain the source address and its corresponding destination address.

Two algorithms are proposed in RISEN. Algorithm 2 is part of algorithm 1. In algorithm 1, if binary bits of source and destination address are the same and if the applicable SE of the first stage (SE_0) and SE of last stage (SE_n) are not faulty. Then request is directly forwarded to the given destination via DEMUX from given source.

### Algorithm 1:
BEGIN
If (S_i and D_i are same)
{
   if (SE_0 and SE_n are not faulty)
   {
      Send request from SE_0 to SE_n;
   }
   else
   {
      Algorithm 2;
   }
}
else
{
   Algorithm 2;
}
End

If the given source (S_i) and destination addresses (D_i) are different then algorithm 2 is used. In algorithm 2, the request is forwarded from given source to the primary switching element (PSE_0) of stage 0. If it is faulty then request is forwarded to first alternate SE (FSE_0) of stage 0. If FSE_0 is also faulty then request is forwarded to second alternate SE (SSE_0). If SSE_0 is
faulty then request will be received by third alternate SE (TSE₀) otherwise send the request to the primary SE of stage 1. If all of the SEs is faulty then drop the request. In the middle stage (k=1 to (n-2)) request is received by the primary switching element (PSEₖ) and if it is faulty then request is received by first alternate SE (FSEₖ). If (FSEₖ) is also faulty then drop the request otherwise send the request to the primary SE of next stage. In the last stage, the request is received by primary switching SE (PSEₙ₋₁). If it is faulty then drop the request otherwise request is forwarded to a given destination through DEMUX.

Algorithm 2:
At Stage 0:
if PSE₀=FB //FB means busy or faulty node
then FSE₀
else if FSE₀=FB
then SSE₀
else if SSE₀=FB
then TSE₀
else if TSE₀=FB
then drop the request
else Send Request to PSE₁
Stage (k=1 to (n-2)):
// where n= \log₂N
if PSEₖ=FB
then FSEₖ
else if FSEₖ=FB
then Drop the Request
else Send Request to PSEₖ₊₁ of Stage k+1
At Stage (n-1):
if PSEₙ₋₁=FB
then Drop the Request
else Send Request to the destination

4 RELIABILITY ANALYSIS AND COMPARISON OF PROPOSED AND EXISTING MINs

In this section, the reliability of IASEN-4 and RISEN is analyzed in terms of upper bound, lower bound of MTTF. Here are some presumptions for the study of the failure rates of the components which are used to evaluate the reliability of MINs:

- The failure rate of a component can be derived from its gate count. For 2×2 crossbar switches, the failure rate is \( \lambda \) (where \( \lambda \) is about \( 10^{-6} \) per hour) [13].
- The failure of \( w \times 1 \) size MUX and \( 1 \times w \) size DEMUX occurs independently and their failure rates are \( \lambda_m \) and \( \lambda_d \) respectively. We assume that the failure rate of \( w \times 1 \) MUX and \( 1 \times w \) DEMUX is \( w\lambda/4 \), i.e. \( \lambda_m = \lambda_d = w\lambda/4 \).

Let the failure rate of 2x3 switching element (SE₂₃) is \( \lambda₃₂ \) and failure rate of 4x2 switching element (SE₄₂) is \( \lambda₄₂ \). Based on the gate counts of the crossbar switch the failure rate of SE₂₃ is \( \lambda₃₂ = 1.5 \lambda \) and the failure rate of SE₄₂ is \( \lambda₄₂ = 2\lambda \). According to the adaptive routing scheme, let us assume that 2×2 size SE in the last stage and its associated 1×4 size DEMUX are in series system. So, we consider these three components as a single segment (SE₂₃). Based on the gate count let the failure rate to this group \( \lambda₃₂ = 3\lambda \).

4.1 Reliability of Proposed MIN (RISEN)

(a) Optimistic or Upper Bound of RISEN

In RISEN, two same size (4×1) MUX are linked to each source and every SE in the first stage has a conjugate pair. For the computation of upper bound, we suppose that RISEN is working as long as one of the two MUX linked to a source in a subnetwork is working and both components in a conjugate pair are not faulty [13][15].

So, we can state that regardless of whether the half of the components or one sub-network is faulty and, even then RISEN is still working. The representation of upper bound of RISEN in terms of block diagram given in Fig. 3.

(b) Pessimistic or Lower Bound of RISEN

To determine the pessimistic or lower bound of RISEN, it is assumed that the RISEN is failed whenever more than one conjugate pair (either switch or loop) has a faulty element or more than one conjugate switch in the last stage fails [13][15].

At the input side of proposed MIN, routing algorithm doesn’t consider the MUX to be an integral part of 3×3 SE [3] [15]. If two MUX are grouped with each SE and assigned them a series system (SE₃ₓ₉). The failure rate of SE₃ₓ₉ is \( \lambda₃₉ = 3.5\lambda \).

As long as at least one of the two MUX attached to a SE is working, the SE can still be used for routing[3][15]. The reliability block diagram of RISEN is shown in Fig. 4.
MTTF$_{RISEN\_LB} =$

### 4.2 Reliability of Existing MIN (IASEN-4)

#### (a) Optimistic or Upper Bound of IASEN-4

For the calculation of upper bound of IASEN-4, we used the same above mentioned procedure that is used to calculate the upper bound of RISEN. The reliability block diagram of MTTF optimistic or upper bound of the IASEN-4 is shown in Fig. 5.

![Upper Bound of IASEN-4](image)

Fig. 5. Upper Bound of IASEN-4

Reliability equations for upper bound MTTF:

\[ f_1 = \left[ 1 - (1 - e^{-\lambda_2})^{N/2} \right] \]
\[ f_2 = \left[ 1 - (1 - e^{-\lambda_2})^{N/4} \right] \]
\[ f_3 = \left[ 1 - (1 - e^{-\lambda_2})^{N/8} \right] \]
\[ f_4 = \left[ 1 - (1 - e^{-\lambda_2})^{N/16} \right] \]

Where, \( \lambda_2 = 2\lambda; \lambda_3 = 3\lambda; \)

\[ R_{IASEN\_4\_UB} = f_1 f_2 f_3 f_4 \]

\[ MTTF_{IASEN\_4\_UB} = \int_0^\infty R_{IASEN\_4\_LB}(t) \]

#### (b) Pessimistic or Lower Bound of IASEN-4

For the calculation of MTTF lower bound of IASEN-4, we applied the same procedure that we used to calculate the MTTF lower bound of RISEN which is mentioned above. The reliability block diagram of lower bound of the IASEN-4 is shown in Fig. 6.

![Lower Bound of IASEN-4](image)

Fig. 6. Lower Bound of IASEN-4

Reliability equations for lower bound MTTF:

\[ f_1 = \left[ 1 - (1 - e^{-\lambda_2})^{N/2} \right] \]
\[ f_2 = \left[ 1 - (1 - e^{-\lambda_2})^{N/4} \right] \]
\[ f_3 = \left[ 1 - (1 - e^{-\lambda_2})^{N/8} \right] \]
\[ f_4 = \left[ 1 - (1 - e^{-\lambda_2})^{N/16} \right] \]

Where, \( \lambda_2 = 2\lambda; \lambda_3 = 3\lambda; \lambda_4 = 3.5\lambda \)

\[ R_{IASEN\_4\_LB} = f_1 f_2 f_3 \]

MTTF$_{IASEN\_4\_LB} = \int_0^\infty R_{IASEN\_4\_LB}(t)$

The results of MTTF reliability equations have been given below in Table 1.

### Table I. MTTF of RISEN and IASEN-4 for Different Network Size

<table>
<thead>
<tr>
<th>Network</th>
<th>MTTF Lower Bound</th>
<th>MTTF Upper Bound</th>
</tr>
</thead>
<tbody>
<tr>
<td>IASEN-4</td>
<td>4.9976</td>
<td>4.9984</td>
</tr>
<tr>
<td>RISEN</td>
<td>4.9947</td>
<td>4.9968</td>
</tr>
<tr>
<td></td>
<td>4.9885</td>
<td>4.9933</td>
</tr>
<tr>
<td></td>
<td>4.9752</td>
<td>4.986</td>
</tr>
<tr>
<td></td>
<td>4.9468</td>
<td>4.9714</td>
</tr>
<tr>
<td></td>
<td>4.8873</td>
<td>4.9412</td>
</tr>
</tbody>
</table>

The comparison graphs of MTTF upper bound and lower bound of existing (IASEN-4) and proposed (RISEN) MINs are shown in Fig. 7 and Fig. 8 respectively.

![MTTF Upper Bound Comparison of RISEN and IASEN-4](image)

Fig. 7. MTTF Upper Bound Comparison of RISEN and IASEN-4

![MTTF Lower Bound Comparison of RISEN and IASEN-4](image)

Fig. 8. MTTF Lower Bound Comparison of RISEN and IASEN-4

### 5 Cost Analysis

In order to estimate the cost of a MIN, it has been assumed that the cost of a switch is proportional to the number of crosspoints within that switch [15]. Therefore, for example, a 2x3 switch has 6 units of hardware cost and 4x1 MUX has 4 units of hardware cost. Thus, RISEN has the cost of N (12+n). The cost analysis for the proposed RISEN and existing IASEN-4 is given in Table 2.

### Table II. Cost Functions for Networks

<table>
<thead>
<tr>
<th>Network</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>IASEN-4</td>
<td>N(7+2n)</td>
</tr>
<tr>
<td>RISEN</td>
<td>N(12+n)</td>
</tr>
</tbody>
</table>

From Fig. 9 it's clear that RISEN and IASEN-4 both are having comparable cost.
7 CONCLUSION
The general objective of designing irregular multistage interconnection networks is high reliability, fault tolerance and good performance even within the presence of faults. We provide a generalized structure (link connection formula for each stage) of RISEN which is rarely discussed in any irregular MINs. RISEN is a progressively re-routable network that gives various paths of variable lengths between a source and destination address. The upper and lower bound reliability analysis demonstrates that proposed RISEN is more reliable than existing IASEN-4. It has been seen that RISEN provides more paths than IASEN-4 between any source-destination pair and it will engage a bigger range of requests even under faults.

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