Design Of Bipolar Signal Integrator Using Voltage To Frequency Converter

Dr. Surya Deo Chaudhary, Jitendra Kumar Saroj

Abstract: This work offers the structure of the bipolar signal integrator by employing voltage to frequency converter. The structure of the bipolar integrator consisting of three functional blocks named as op-amp, absolute value circuit and up/down counter. The conversion of bipolar signal to monopolar signal is performed by using absolute value circuit. Then the converted signal is further converted to a frequency by means of VFC and counted over a well-known sample periods. This offers the whole count equivalent to the time integral of the certain signal. The necessity for expensive, low leakage op-amps, low drift and capacitors found in analog integrators. The structure of the circuit is simulated on Cadence virtuoso Design Environment employing SCL 180 nm transistor model with the required power supply (1.8 v). The dissipation of the power in the circuit is 876 µw.

Keywords: Op-amp, converter, integrator, VFCs and up/down counter.

1. INTRODUCTION

Fundamentally an integrator is an electronic element who has signal is basically time integral of the input signal[1]. An integrator is basically an A/D converter with a long inspecting period. Reconciliation is a significant piece of many building and logical applications. The integrator circuits are for the most part utilized in simple PCs, ADC, wave moulding circuits and logical estimation. The sign to be incorporated is changed over to a recurrence utilizing VFC and tallied up/down counter as appeared in Fig. 1. The complete count is equivalent to the time integral of the signal visualized in the equation (1).

$$\int V\,dT = K \int F\,d\,T = KN \qquad \ldots(1)$$

Where N= Total count

And K= VFC Scaling Constant

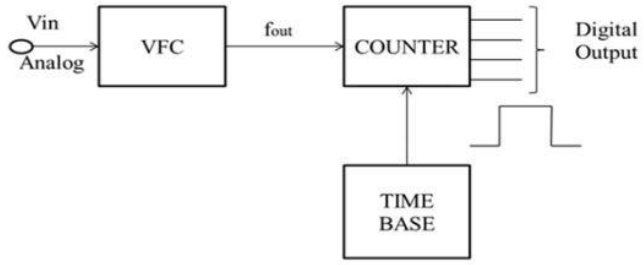


Fig. 1. Voltage to frequency converter based on ADC

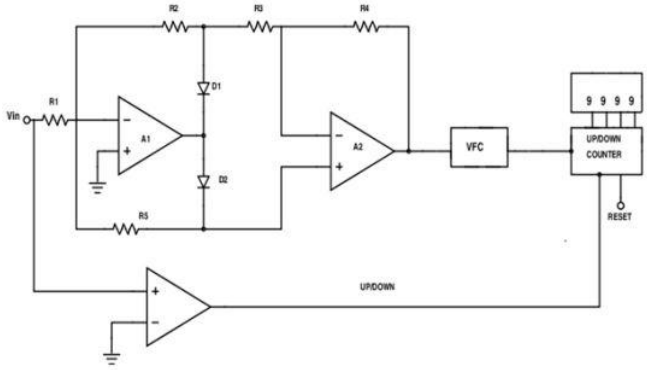
Analog integrators are very inexpensive and easy for the time factors from 1 milli-seconds to hundred seconds[2]. But as the time constants approaches 1000 seconds, the total expenditure of the operational amplifiers improves. This results increase in the overall cost of the analog integrator so that of the voltage to frequency integrator turn into a tremendously striking alternative.

- *Dr. Surya Deo Chaudhary; Department of Electronics & Communication Engineering, Noida Institute of Engineering and Technology researchnietip@gmail.com*
- *Jitendra Kumar Saroj; Department of Electronics & Communication Engineering, Noida Institute of Engineering and Technology researchnietip@gmail.com*

In addition with the capability to integrate over long duration of periods, the VFC A/D converter [3]system is visualized in figure having the below stated advantages.

- The designer can control the conversion speed and resolution of the proposed system.
- When integrated with the sample period wide than the noise period then the noise rejection is performed.
- The output of the system can be directly interfaced into the digital information-processing system, deployed for the display (preferably seven segmented display) or reverted back to the analog with low cast D/A converter.
- The process may be intermittent without distressing the integrated value.
- The digital counter may be pre-set to any of the desired value before integrating down or up.

2. CIRCUIT DESCRIPTION

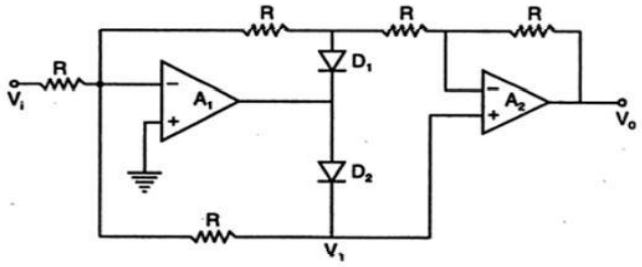


The elementary structure block of the integrator are

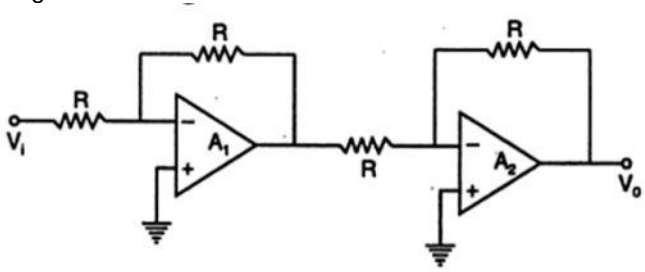
- Absolute Value Circuit
- Voltage to Frequency Converter
- 4 bit Up/Down Counter

I. ABSOLUTE VALUE CIRCUIT

An absolute value circuit is basically a full wave rectifier[4]. The structure of the absolute value circuit is as shown in the below figure 4. The positive input voltage affects as a unity gain inverter. The next amplifier inverts the output of the first amplifier to generate a positive output voltage.



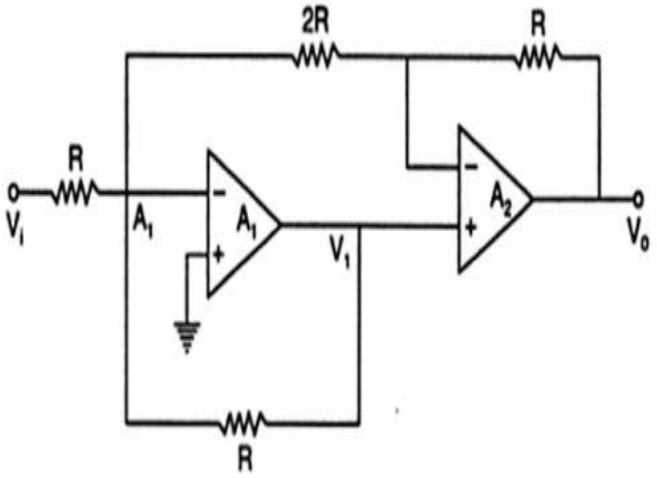
When input voltage Vi is positive, D1 will be forward biased and hence D1 conducts. D2 will be reversed biased hence D2 will not conduct. We can draw equivalent circuit as stated in the figure below:



A1 and A2 act as inverter by a gain of unity. Thus the output of the circuit is as similar as input

VO = Vi

When input Vi is negative, D1 is in OFF state whereas D2 is in ON state. In ON state. In particular case, the equivalent circuit may be sketched as



Stating Kirchhoff's current law at the input node of employing ideal op-amp parameters for A1 and A2, the sum of the current entering to the node A should be zero i.e.

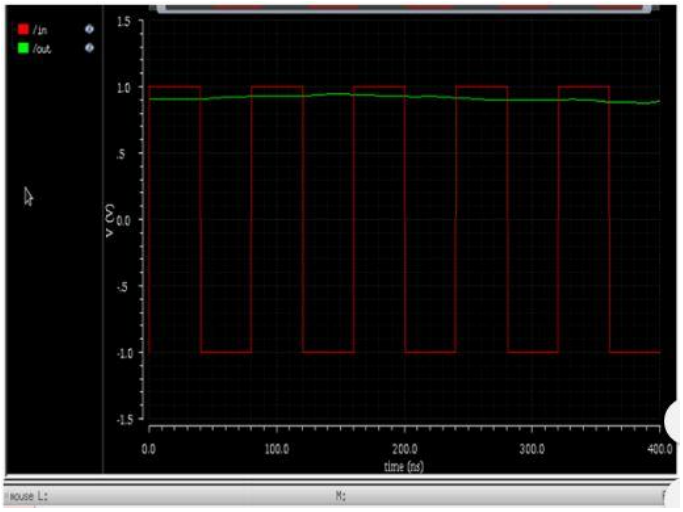
$$\frac{Vi}{R}+\frac{V1}{R}+\frac{V1}{R}=0$$

$$V_1=-\frac{2}{3}V_i$$

$$V_0=(1+\frac{R}{2R})(-\frac{2}{3}V_i)$$

$$V_0=-V_i$$

For the negative input, the output will be positive. Therefore the output attained from the circuit will always be positive for negative or positive inputs. For simulation of the resistance value of the every resistor taken i.e. 10 KΩ and the supplied power is VDD=1.8V.



II. VOLTAGE TO FREQUENCY CONVERTER

A voltage to recurrence converter is an information converter whose yield recurrence is corresponding to the info voltage. In some nonlinear VFCs, yield recurrence might be corresponding to square base of the info voltage or exponentially identified with the information voltage. VFCs are not the same as voltage controlled oscillators (VCO)[5] as far as various execution details, for example, soundness with temperature and supply voltage, wide unique range and low linearity mistake. The old style square chart of voltage to recurrence converter is appeared in Fig. 1.4.

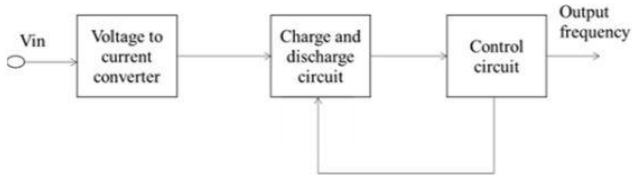
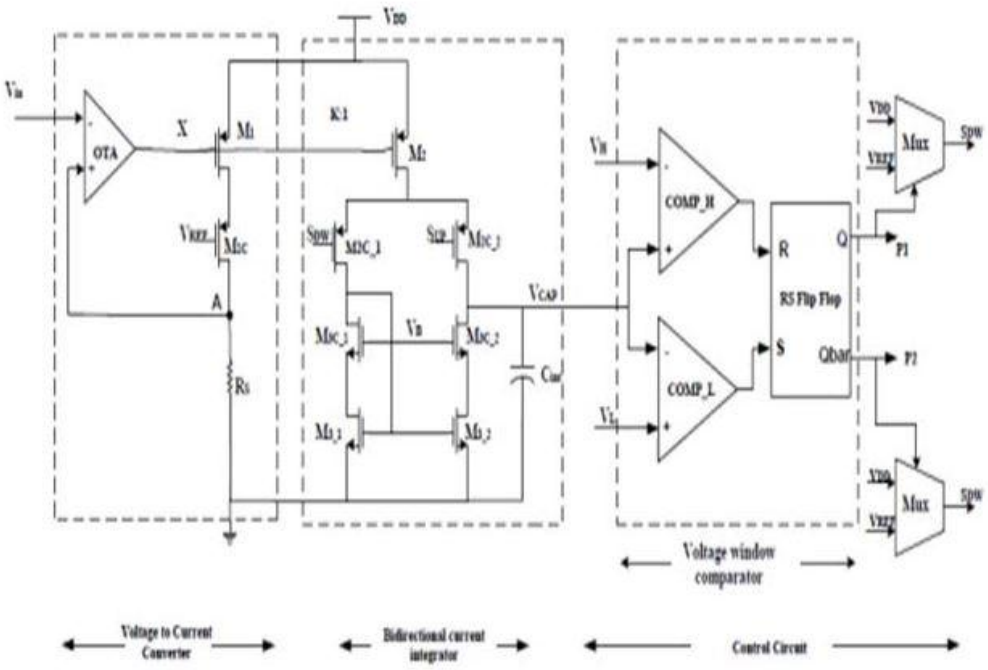


Fig. 2: block diagram of voltage to frequency converter

The VFC essentially consisting of voltage to current converter, charging and discharging circuit and a control circuit that controls the charging and discharging of the circuit.

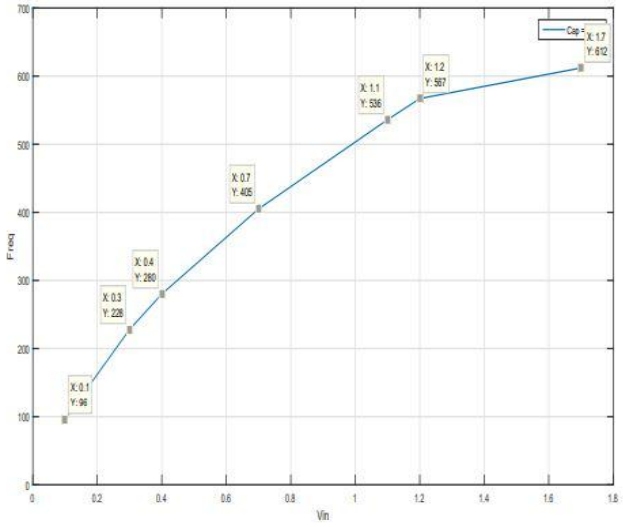
The proposed structure as shown in the figure below:



The signal voltage is changed over into a current by utilizing voltage to current converter. This current is reflected into bidirectional current integrator. The reflected current on the other hand charges and releases the incorporating capacitor Cint between the points of confinement VH and VL of voltage window comparator. The charging and releasing is constrained by exchanging sign SUP and SDW created by the voltage window comparator. At the point when compasses VH, the yield of upper comparator (COMP_H) goes to '1', which resets the RS flip[6] failure. This outcomes in P1=0, P2=1, SUP=VDD and SDW= Vref. Also, the capacitor release stage starts. At the point when Vcap comes to VL the yield of lower comparator (COMP_L) goes to 1, which sets the RS flip. This outcomes in P1=1, P2=0, SUP=Vref and SDW=VDD and the capacitor charging stage starts. Along these lines, a progression of heartbeats are created at a rate relative to enter voltage. The yield recurrence of the VFC is given by

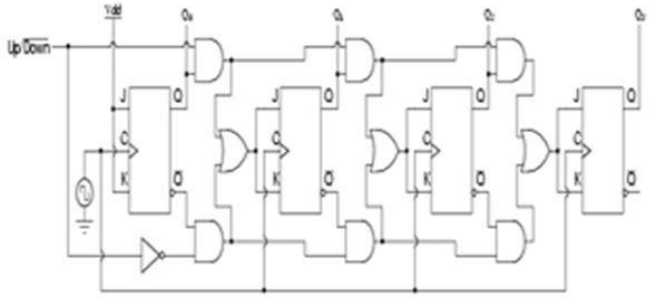
$$f_0 = \frac{1}{2C_{int}(V_H - V_L)} \frac{V_{in}}{KR_S}$$

The sign waveform at the yield of VFC and over the capacitor Vcap at information voltage Vin =0.6 V are appeared in Fig. beneath, which demonstrates that the voltage over the capacitor changes directly between as far as possible VH and VL. The exchange qualities of the VFC is appeared in Fig.



III. UP/DOWN COUNTER

A synchronized 4-bit up/down counter constructed from JK flip flops is visualized in the figure. Contingent on the logic value to the Up/Down input, the counter will increase or decrease its value on falling edge of the clock signal[7].



3. WORKING OF BIPOLAR SIGNAL INTEGRATOR

A straight forward absolute circuit and a counter converts the VFC into a bipolar signal integrator. Total worth circuit yields the positive voltage whether input voltage is negative or positive. At that point VFC changes over this positive voltage into some frequency. Comparator chooses the counting mode of up/down counter.

The output of the counter is given by

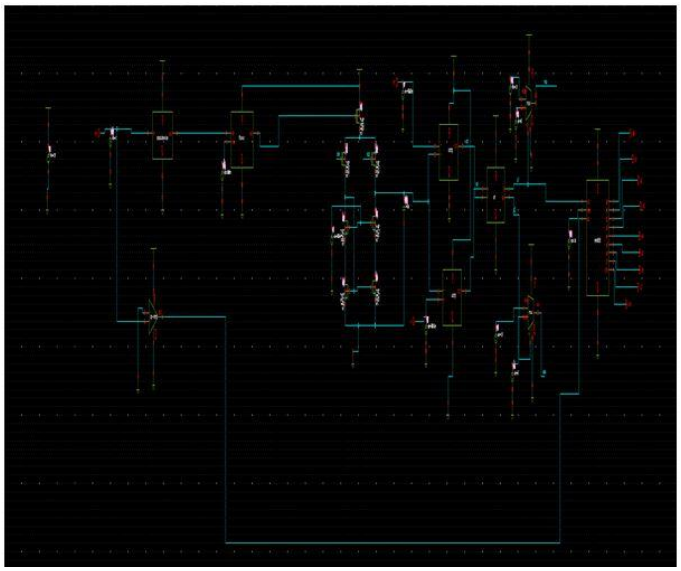
$$\int V\,dT = K \int F\,d\,T = KN \quad \ldots(1)$$

Where

N is the number of pulses.

F is the output frequency of the VFC.

The frequency from the voltage converter changes linearly from 0 to 1.2 MHz above input range of 0-1.2 volts. The counter is employed that counts the pulses 8 bit up/down.



4. CONCLUSION

The total number of output pulses is equal to integration of the input signal. The analog integrators are inexpensive and easy for the time constants from the milliseconds to hundred seconds. As the time constant reached to the thousand seconds, the operational amplifier cost will increases. This results the increase in overall cost of the analog integrator so that the voltage to frequency integrator turn into eye-catching alternative.

REFERENCES

[1] O. Gassmann, K. Frankenberger, M. Csik, O. Gassmann, K. Frankenberger, and M. Csik, “Integrator,” in Geschäftsmodelle entwickeln, 2017.

[2] B. Razavi, “The Switched-Capacitor Integrator [a Circuit for All Seasons],” IEEE Solid-State Circuits Mag., 2017.

[3] Y. K. Ramadass and A. P. Chandrakasan, “Voltage scalable switched capacitor DC-DC converter for ultra-low-power on-chip applications,” in PESC Record - IEEE Annual Power Electronics Specialists Conference, 2007.

[4] I. AspenCore, “Full Wave Rectifier and Bridge Rectifier Theory,” Copyright © 2017 by AspenCore, Inc., 2017. .

[5] J. G. Webster, F. Vidal-Verdú, R. Navas-González, M. Delgado-Restituto, and Á. Rodríguez-Vázquez, “Voltage-To-Frequency Converters,” in Wiley Encyclopedia of Electrical and Electronics Engineering, 2018.

[6] H. Korhonen and S. P. Järvinen, “Active Longitudes and Flip-Flops in Binary Stars,” Proc. Int. Astron. Union, 2006.

[7] L. A. Dinnebeil, “Top-Down and Bottom-Up,” Young Except. Child., 2014.