Design Of Speed & Area Efficient NoC Architecture By Integrating Switches With Simplified Decoder And Reduced Buffers

Vivek tiwari, Kavita khare

Abstract -Network-on-Chip is used to integrate large numbers of Intellectual Property blocks on a single Integrated Chip. NoC router is one of the important parts of networking that is used inside a Chip. In this paper a new NoC router architecture is proposed which consist of firstly a modified crossbar switch secondly eight 8 bit buffers instead of sixteen bit 8 buffers at input and output channel and thirdly modified decoder which is a part of arbiter of NoC router. Proposed NoC Router design reduces area by 3% and delay by 1.39% as compared to conventional NoC router. It is also proposed and analysed here that, new NoC architected if integrated with conventional NoC architecture shows 17.24 % of area saved for 4x4, 8x8, 16x16 and 32x32 meshes NoC architecture when compared with conventional NoC architecture. Proposed NoC Architecture model is simulated in Xilinx ISE 9.2i and target device is Virtex4.

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I.INTRODUCTION

To provide appropriate communication between cores of multi-core chip Network on chip (NoC) is a more reliable way to full fill high performance computing requirements. Network on Chip consist NoC routers and various link to connect them. There are various mesh and torus based topologies to connect all routers with each other [1]. Between two routing techniques deterministic and adaptive routing techniques, deterministic technique where X-Y routing is most popular. Programmable and adaptive NoC router is used as per requirement of new general purpose multi cluster chips. [2].

A deterministic conventional NoC router architecture consist of input output channel, buffer, crossbar switch, MUX, decoder, X-Y router and arbiter[3].

There are several existing area and power efficient NoC architectures [5].Crossbar switch and input output channel used in NoC router is designed to reduce area, power and delay in BiNoC and input output configurable NoC router [6-7].Our proposed work focuses on modification of architecture of crossbar switch and decoder with input output channels of NoC router to make it area and time efficient.
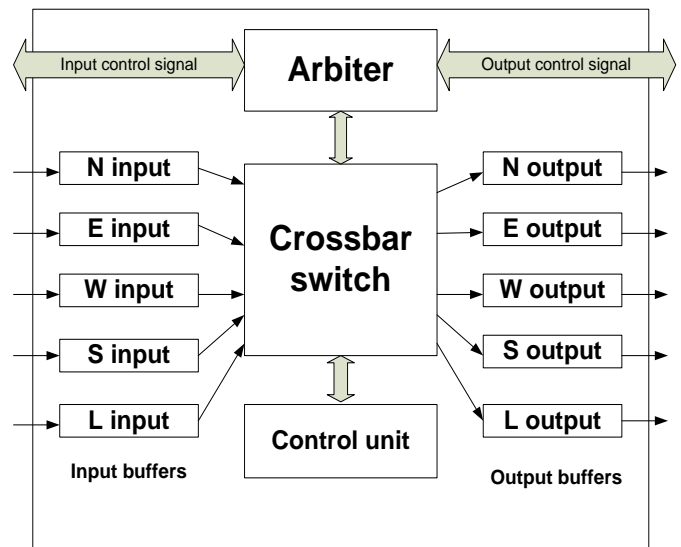.

Figure 1 : Conventional NoC router architecture

II-RELATED WORK

conventional NoC router architecture consist of components namely (i) input output channel with buffer (ii) crossbar switch (iii) arbiter (iv) X-Y router as shown in figure 1. This NoC router consist of five input and five output channel i.e. north, south ,east, west, local input output channel. Each channel is connected with its neighbouring channel through physical channel (link).

Router's main function is to route data from each input channel to appropriate output channel, to forward data towards final destination.

To perform above function router has an input buffer at each input port, a 5x5 crossbar switch for connecting input channel to output channel and some control logic circuit to ensure correct routing[6], [7].

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Components of conventional NoC router

Input/output Ports

A conventional NoC router architecture it consist of input/output ports where both consist of infifo , outfifo , and xy router, where buffer of each channel consist of 16 eight bit buffers[8].

Crossbar switch

Crossbar switch is used to connect five input channel to five output channel it consists lots of switches which arranged in the form of matrix organization[9]. Input and output link of crossbar switch arranged in the form of row and column lines. They arranged in such a way that they crosses each other and switches are placed at their crossing point to establish connectivity between them. Crossbar switch is a non blocking type switch i.e. it does not interfere any other input output connection. In any NoC router crossbar switch and input output channel is main area and power contributor [10], [11],[12],[13],[14],[15].

Arbiter

Arbiter allocates a time slot of the cross-bar switch to move flits from an input channel to an output channel. In a conventional NoC, has an equal number of input lines and output lines and its output is the grant signal as discussed in [16].A conventional NoC Router architecture [17] is simulated in Xilinx9.2i and its simulation results is shown in **Error! No bookmark name given.**Figure- 2.
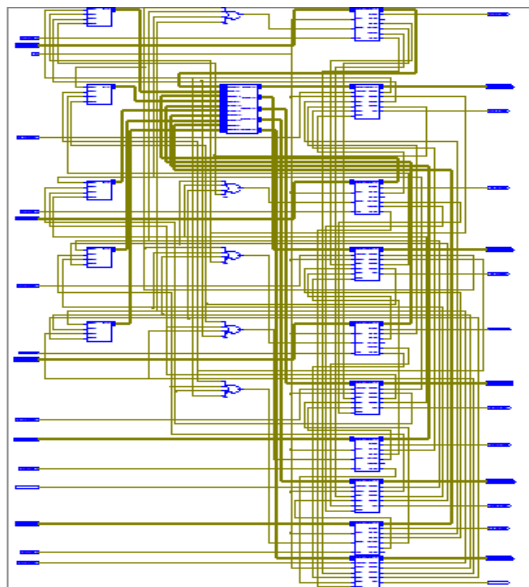

Figure 2 RTL view of conventional NoC router architecture

Present work proposes a NoC architecture with certain benefits

- Modified Crossbar switch acquires less area (less number of LUTs) as compared to conventional NoC router [8], [17]–[20]

- Decoder which is part of Arbiter is modified with less complexity and area when compared to conventional NoC router [8], [17]–[20]
- Eight 8 bit buffers at input and output channel in contrast with sixteen 8 bit buffers of conventional NoC.

III. PROPOSED NOC ROUTER ARCHITECTURE

In proposed NoC router architecture has a input channel ,output channel, crossbar switch, arbiter, X-Y router, decoder, infifo, outfifo such as conventional NoC Router architecture[17].as shown in Figure-3.
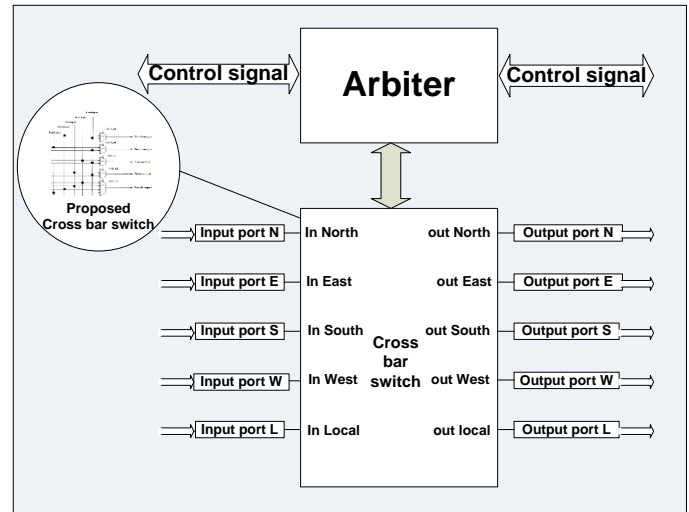

Figure 3 Proposed NoC Router architecture

In proposed NoC router architecture a conventional crossbar switch, which consist five 4x1 MUX is replaced by a new crossbar switch as shown in Figure-4. New crossbar switch consist of four 2x1 MUX and one 4x1 MUX. Due to this new crossbar structure there is a significant improvement in number of LUT as compared to conventional crossbar switch that is used in conventional NoC router architecture[17].
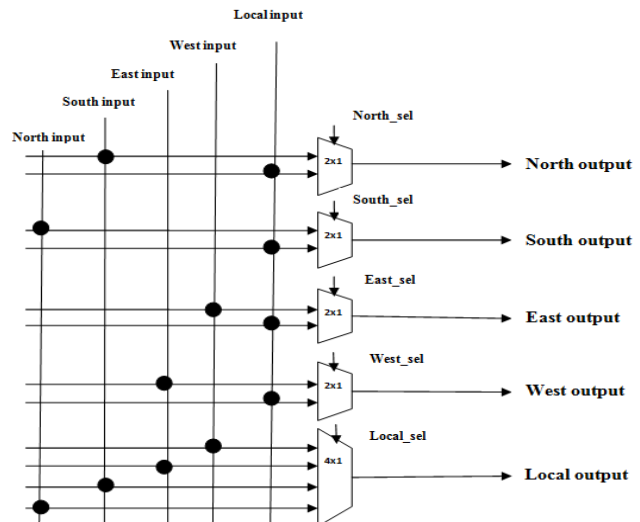
Figure 4 Block diagram of proposed crossbar switch

- Decoder circuit is shown in figure-5 is used in conventional NoC router architecture to select one selection line request among the four upcoming input data transfer request [17]. This kind of five 4x2 decoder is used in conventional NoC router architecture. In proposed NoC router architecture these five decoders are replaced by a simple 2 input 1 output OR gate circuit as shown in Figure-6.
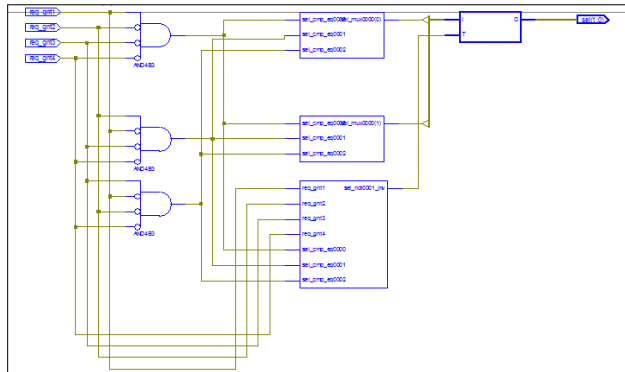

Figure 5 RTL view of Decoder circuit used in conventional NoC router architecture
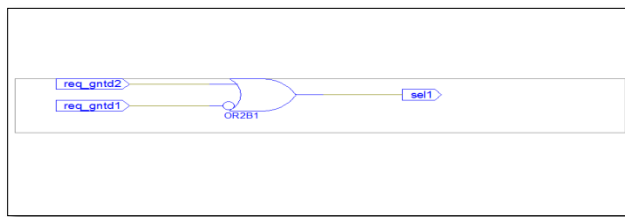

Figure 6 RTL view of Proposed new 2 input 1 output are gate in place of Decoder circuit.

This proposed logic gate also use less number of LUTs as compares to decoders used in conventional NoC. And contribute to reduce total number of LUTs as compared to conventional NOC.

Infifo, Outfifo circuit is used in input channel and output channel of NoC Router. Sixteen 8 bit memory spaces available in conventional NoC Router architecture whereas in proposed eight 8 bit memory spaces are used. Figure-7 and Figure-8 shows RTL view of infifo used in conventional and proposed NoC router architecture [17].
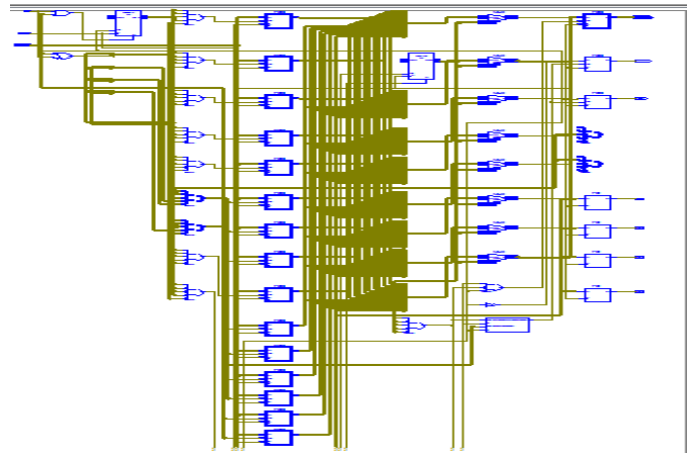

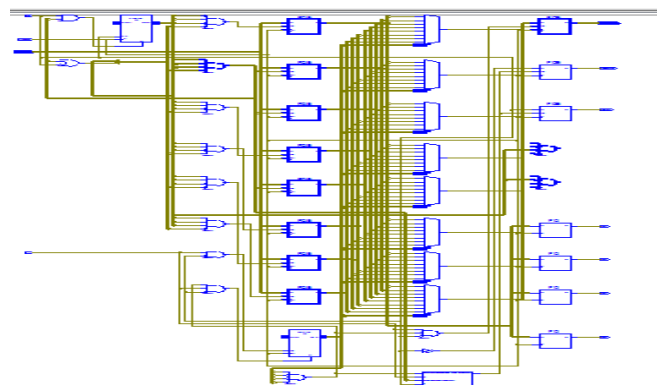Figure 7 RTL view of infifo used in conventional NoC router architecture

Figure 8 RTL view of proposed infifo used in Proposed NoC router architecture

Due to improved crossbar switch design. It requires only eight 8 bit memory slots instead of sixteen 8 bit memory slots. At four input port and four output ports i.e. north input output port, south input output port, east input output port, and west input output port. Only at local input and output channel it uses sixteen 8 bit memories. Since proposed router uses only 8 eight bit memory locations at four inputs outputs channel. It significantly reduces total number of memory locations as compare to conventional NoC router.

By incorporating all proposed individual circuit i.e. new crossbar switch, new simplified decoder circuit, new buffer into a NoC router, we get a very efficient and effective NoC router. Which consume less number of LUTs units as compare to conventional NoC router.

IV. RESULT

Design of proposed NoC router architecture has been synthesized and simulated on Xilinx9.2i virtex4 FPGA Device. RTL view and simulation result of proposed method is shown in Figure.11, Figure.12 and Figure.13 simuntanously. Figure.11 shows RTL view of Proposed NoC architecture, figure.12 shows the schematic view of the proposed NoC router architecture and Figure.13 shows the results of switching of input to the output at different control signals in the form of wave. Table.1 shows that proposed NoC router architecture required only 589 number of 4 input LUTs as compared to 899 total numbers of 4 input LUTs required for

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conventional NoC router architecture. It is also shown in table.1 that 3% less LUTs required in proposed architecture compare to conventional architecture. RTL view decoder circuit is shown in figure.5, which used in conventional router. A less complicated circuits RTL view is shown in Figure.6, which is proposed in this work. The limitation of proposed new NoC architecture when it is implemented in 4x4 mesh architecture is that some of its nodes are not able to receive data from their neighbouring nodes due to straight data transfer feature of proposed NoC router. For optimum performance of this router and to make a mesh NoC structure efficient, it is proposed that it should be used in integration with conventional NoC router. 4x4 mesh architecture only with conventional NoC router and in proposed manner is expressed in Figure-12 and Figure-13 In Table.2 a comparative analysis between proposed   and conventional 4x4, 8x8, 16x16 and 32x32 meshes architecture is shown, which shows that proposed mesh structure required 17.24% less number of LUTs as compared to conventional architecture.

TABLE 1:

UTILIZATION OF FPGA RESOURCE BY CONVENTIONAL AND PROPOSED NOC ROUTER ARCHITECTURE (SELECTED DEVICE-VIRTEX4)

Resource Available		Conventional NoC Router architecture		Proposed NoC Router architecture	
		Used	Utilization	Used	Utilization
Slice	6144	812	13%	426	6%
Slice flip-flops	12288	895	7%	555	4%
LUTs	12288	899	7%	589	4%
I OBs	240	101	42%	101	42%
GCLKs	32	1	3%	1	3%

TABLE.2

UTILIZATION OF AREA (NUMBER OF LUT) BETWEEN CONVENTIONAL MESH ARCHITECTURE AND PROPOSED MESH ARCHITECTURE

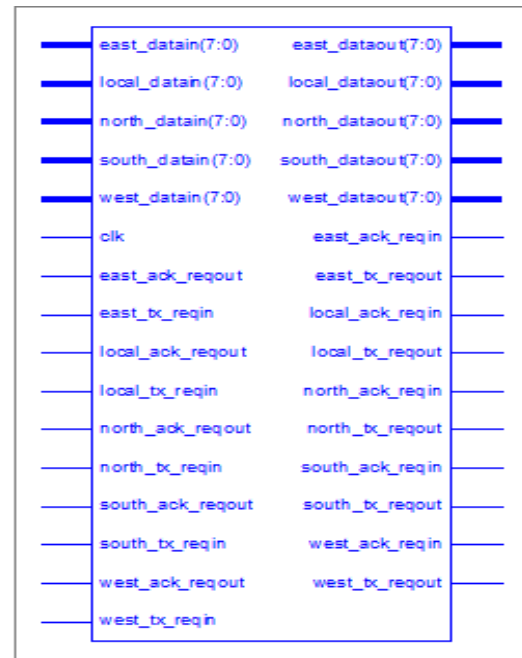| Mesh	Conventional NoC Router(total LUT)	Proposed NoC Router(total LUT)	% of less LUTs required
4x4	14384	11904	17.24%
8x8	57536	47616	17.24%
16x16	230144	190464	17.24%
32x32	920576	761856	17.24%

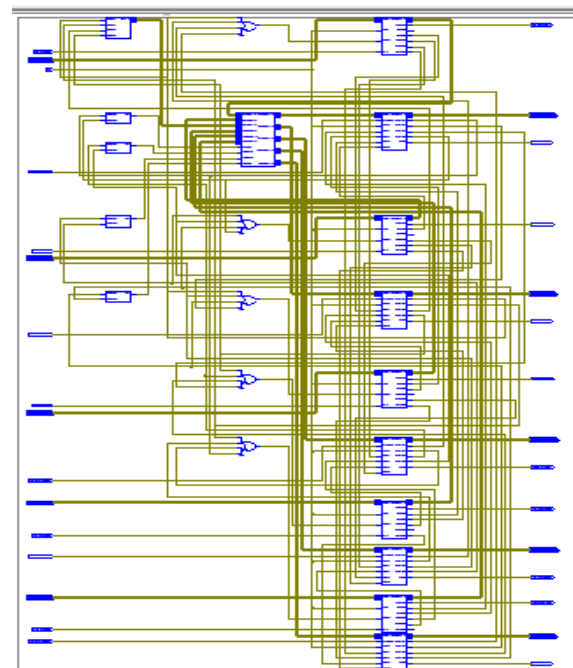Figure.9: RTL view of proposed memory less NoC router design

Figure.10: Schematic of proposed memory less NoC Router architecture design.
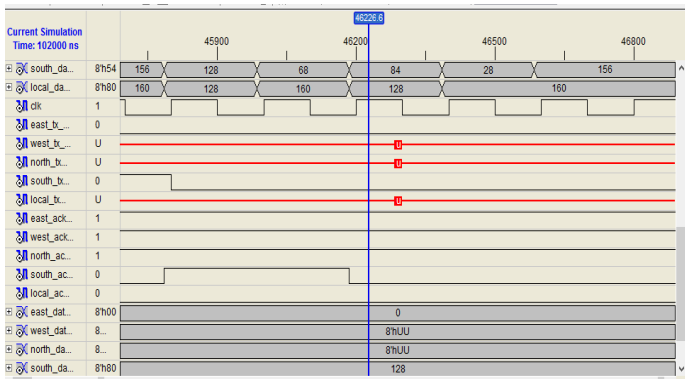
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Figure 91: Simulation result for proposed memory less NoC Router design
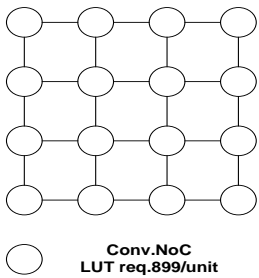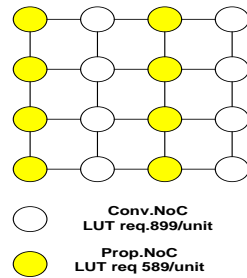

Figure.12   Figure.13

Figure.12 4x4 NoC architecture with conventional NoC router. Figure.13 shows NoC architecture which has integration of conventional and proposed switches.

V. CONCLUSION

In this paper a new NoC router architecture with an efficient crossbar switch, simplified decoder circuit and less number of buffer at input channel and output channel is proposed, which significantly reduce area (number of LUTs) by 3% and delay by 1.39% as compared to conventional NoC router. A combinational n x n mesh architecture, which consist both conventional and proposed architecture in parallel manner is proposed. 4x4, 8x8, 16x16 and 32x32 combinational mesh architecture are analysed and compared with conventional architecture. This analysis shows that proposed mess structure uses 17.24% less number of LUTS as compared to traditional mesh architecture.

VI. REFRENCES

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Vivek Tiwari received B.E (Electronics and Communication) in 2007 From BCE Mandideep, Bhopal and M.Tech in 2011 with specialisation in VLSI and Embedded System fromTIT Bhopal, Currently he is pursuing part time PhD in Electronics and Communication in MANIT, Bhopal. Network on-Chip (NoC), Reliability and Modelling and Simulation. He is currently an assistant professor in SIRTS Bhopal.

Kavita Khare received the B.Tech degree in Electronics and Communication Engg. In 1989, M.Tech. degree in digital communication systems in 1993, and the Ph.D. degree In the field of VLSI design in 2004.Currently, she is working as Professor in Electronics and Communication Engineering in MANIT, Bhopal, India. Her fields of interest are VLSI design and communication systems. Her research mainly includes Design of arithmetic circuits and various communication algorithms related to synchronization, estimation and routing. She has nearly 150 publications in various international conferences and journals.