Solar-Powered Multilevel Inverter With A Reduced Number Of Switches

A S Kamaraja, K Priyadharshini

Abstract: In this paper proposes renewable energy application based multilevel topology is introduced to reduce the number of elements in the circuit and improve the quality of output in a photovoltaic application. A large amount of output level obtained with the proposed binary asymmetric configuration. Desired switching pulses are generated using a trapezoidal reference with a triangular carrier wave. The proposed system requires nine switches to produce 63-level output voltage with Total Harmonic Distortion of 2.74% without any filters. The value of total harmonic distortion satisfies the IEEE Standards. The proposed MLI will be tested with the help of MATLAB/SIMULINK environment.

Index Terms: Multilevel inverter, Pulse width modulation, Trapezoidal waveform, Total Harmonic Distortion, Photovoltaic panels, MATLAB/SIMULINK

1INTRODUCTION

The multilevel inverter has many advantages compared to conventional two-level inverters such as high voltage capability and lower switching losses and produces the high-quality output [1]. Due to more number of advantages multilevel inverters are used medium and high power applications [2]. Normally diode clamped multilevel inverter (DCMLI), Flying capacitor multilevel inverter (FCMLI), H-bridge multilevel inverters are traditionally used in many applications [3].In modern days hybrid multilevel inverters are used to obtain more power but the number of components will be increased the total number of components are directly proportional to the number of levels. FCMLI and DCMLI are having voltage across DC bus capacitor id difficult one and it makes circuit complexity and larger in size [4]. Less number of components has its own advantages and disadvantages. In Refs. [5-20] the bidirectional switches are configured to achieve the desired voltage level. In Refs. [21-25] conventionally transformers are used to generate a higher output voltage. Usage of transformers the system will be very bulky and less life span. In this paper, the number of switches is reduced without any bidirectional switches and transformer. Therefore, the proposed topology has low cost as well as size. The proposed topology requires only 9 switches to produce a 63-level output voltage with a Total Harmonic Distortion of 2.74%.

2 PROPOSED METHODOLOGY

In this topology is built using the combination of power semiconductor devices. The proposed multilevel inverter topology is shown in Fig 1a. The switches and DC voltage source combination is in parallel with the bypass diode. It has two operating modes. When the switch T1 is on state, voltage appears across the diode D1 is Vdc1. Hence the value of output voltage is 2Vdc (Vdc1+Vdc2). When the switch T1 is in off state, the bypass diodes are conducts to generate the Vdc output voltage.

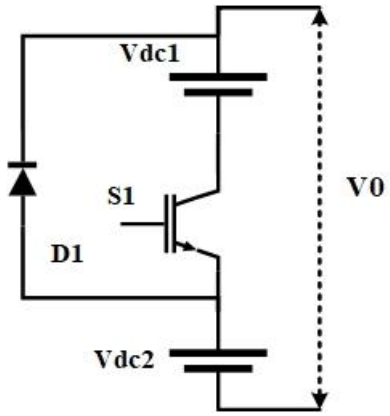

Fig 1a: Basic Structure of proposed topology

For generating the output voltage, the highest number of cascading connection of multilevel inverter levels is needed. When compared to asymmetric inverter, symmetric inverters produce minimum level of the output voltage. Figure1b shows the proposed topology of multilevel inverter for generating a 63-level output voltage. The binary sequence ratio is 1:2:4:8.The desired output voltage level is produced by a combination of H-Bridge inverter and reduced switch configuration. The generalized formula for multilevel inverter configuration is shown in Table I. The proposed topology for generating 63-level output voltage in both positive and negative sequences is shown in Table2.

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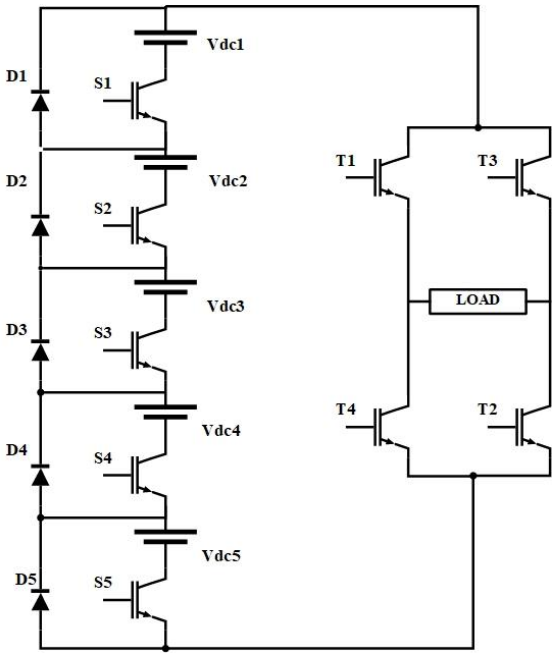

Fig 1b: Proposed Configuration

TABLE I Different parameters used for proposed multilevel inverter

Quantity	Values
Dc Sources	2n where n = 0, 1, 2...
Ratio of DC Sources	1:2:4:8
Number of Switches	k + 4
Number of DC Sources	k
Number of Diodes	k + 4
Number of Driver Circuit	k+4
Number of level	2k+1 - 1

3 MODULATION TECHNIQUES

Pulse width modulation is an effective technique for controlling the multilevel inverter output voltage. Normally sinusoidal pulse width modulations are used to achieve the desired output voltage. The proposed topology switches are triggered by using the trapezoidal reference with a triangular carrier wave. This technique provides better performance output voltage compared with the sinusoidal pulse width modulation technique. The combination of two slopes and one horizontal line makes the trapezoidal reference waveform. Generally, triangular reference waveform attained by limiting the magnitude value of the waveform. The angle horizontal line of the waveform will be

$$2\Phi = (1-\sigma)\,\pi \qquad (1)$$

Where σ is called as the triangular factor.
If the triangular factor is σ=1, the waveform shape will be triangular. The shape of the waveform is purely depending on the location of the slope angle (α). Fig 2 shows the various angle of slope for the triangular waveform. A mathematical formula for calculating the different slope of a different order is given by

$$A_n=\frac{4}{\pi}\int_0^{\frac{\pi}{2}} F(\theta) sin\, n\theta\, d\theta \qquad (2)$$

Where

$$F(\theta) = \begin{cases} \frac{1}{a}\ 0 < \theta < 90 \\ 1\ \alpha < \theta < 90 \end{cases} \qquad (3)$$

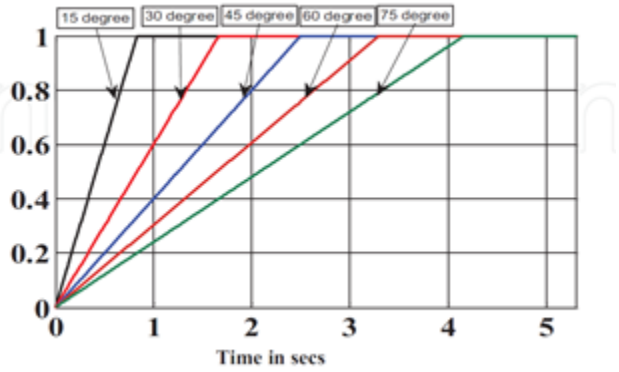

Fig 2: Trapezoidal References of Various slope angle

If the slope angle moves towards 90 degrees, the harmonic order value decreases. Fig 3 shows the different harmonic orders for different slope angles. In this paper, the slope angle will be considered as 60 degrees.

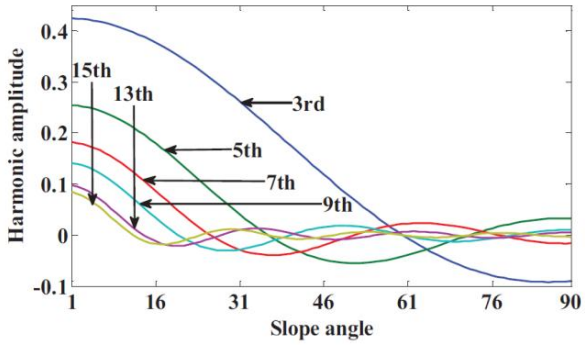

Fig 3: Different harmonic orders for different slope angles

In this paper unipolar reference is considered for generating the switching pulses.

Table II Switching states of the proposed configuration

States	Switching states	Output voltage	States	Switching states	Output voltage
1.	S1,D2,D3,D4,T1,T2	Vdc	16.	S1,D2,D3,D4,T3,T4	-Vdc
2.	S2,D1,D3,D4,T1,T2	2 Vdc	17.	S2,D1,D3,D4,T3,T4	-2 Vdc
3.	S1,S2,D3,D4,T1,T2	3 Vdc	18.	S1,S2,D3,D4, T3,T4	-3 Vdc
4.	S3,D1,D2,D4,T1,T2	4 Vdc	19.	S3,D1,D2,D4,T3,T4	-4 Vdc
5.	S1,S3,D2,D4,T1,T2	5 Vdc	20.	S1,S3,D2,D4,T3,T4	-5 Vdc
6.	S2,S3,D1,D4,T1,T2	6 Vdc	21.	S2,S3,D1,D4,T3,T4	-6 Vdc
7.	S1,S2,S3,D4, T1,T2	7 Vdc	22.	S1,S2,S3,D4,T3,T4	-7 Vdc
8.	S4,D1,D2,D3,T1,T2	8 Vdc	23.	S4,D1,D2,D3,T3,T4	-8 Vdc
9.	S1,S4,D2,D3, T1,T2	9 Vdc	24.	S1,S4,D2,D3,T3,T4	-9 Vdc
10.	S2,S4,D1,D3, T1,T2	10 Vdc	25.	S2,S4,D1,D3,T3,T4	-10 Vdc
11.	S1,S2,S4,D3,T1,T2	11 Vdc	26.	S1,S2,S4,D3, T3,T4	-11 Vdc
12.	S3,S4,D1,D2,T1,T2	12 Vdc	27.	S3,S4,D1,D2,T3,T4	-12 Vdc
13.	S1,S3,S4,D2,T1,T2	13 Vdc	28.	S1,S3,S4,D2,T3,T4	-13 Vdc
14.	S2,S3,S4,D1,T1,T2	14 Vdc	29.	S2,S3,S4,D1,T3,T4	-14 Vdc
15.	S1,S2,S3,S4,T1,T2	15 Vdc	30.	S1,S2,S3,S4,T3,T4	-15 Vdc
16.	S1,S2,S5,D5,T1,T2	16Vdc	31.	S1,S2,S5,D5,T3,T4	-16Vdc

4 PROPOSED METHODOLOGY INTEGRATED WITH PHOTOVOLTAIC PANELS

The proposed topology needs 5 separate DC sources to generate the output voltage, so the separate DC sources are replaced by the photovoltaic panel. In this paper, a 100W solar panel is considered. Fig 4 shows the proposed topology integrated with a solar panel.

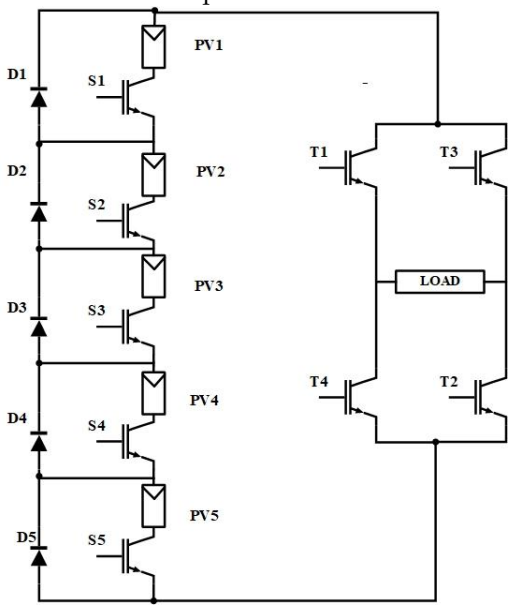

Fig4: Proposed topology integrated with photovoltaic panels

For a conventional type solar panel integration requires high gain converters and separate MPPT technique for achieving the required output voltage. So, the system will be very bulky and complexity.

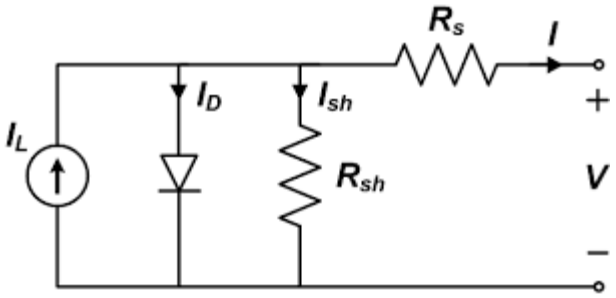

Fig5: Single-diode model a practical photovoltaic cell

Table III Parameters of Photovoltaic cell

Parameters	Values
Max. Power (Pm)	100W
Voltage at max. power (Vmp)	17V
Current at max. power (Imp)	8.24A
OC voltage (Voc)	21V
SC current (Isc)	10A
coefficient of temp(Ki) of Isc	(0.065± 0.015)%/°C

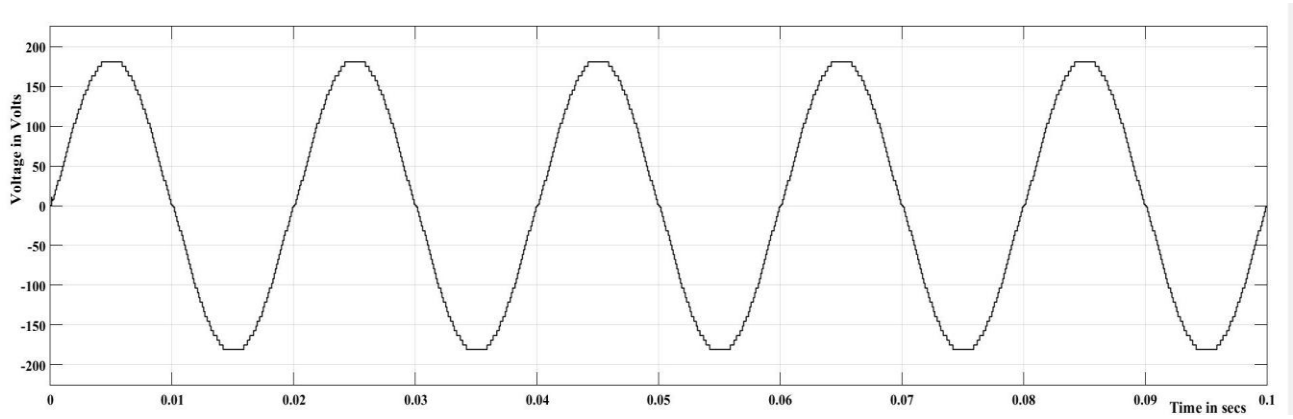

Fig6: Simulation Results of output voltage

Table IV: Components requirements for various topologies

Inverter Type/Components	DCMLI	FCMLI	CHBMLI	Proposed MLI
Requirement of switches	60	60	60	9
Driver circuits	60	60	60	9
Clamping Diodes	56	-	-	-
Clamping capacitors	-	28	-	-
DC bus capacitors	30	30	-	-
Number of switches/diodes per voltage level	30	30	30	6

In order to reduce the complexity, the solar panels are series-connected to achieve the required output voltage. Fig5 shows the single equivalent circuit for a single photovoltaic cell. Table III shows the different parameters used to design a photovoltaic cell.

5 SIMULATION RESULTS AND DISCUSSION

The proposed MLI topology tested with SIMULINK for generating the 63-level output voltage with trapezoidal pulse width modulation to produce a better harmonic profile and reduce the carrier count with the help of the PWM strategy.Fig6 and Fig7 show the output voltage and harmonic profile of a proposed MLI topology. Table IV shows the comparison of proposed topology with conventional MLIs in various factors. From Table IV it is clearly understood the proposed topology requires a minimum count of switches to produce the desired output voltage.

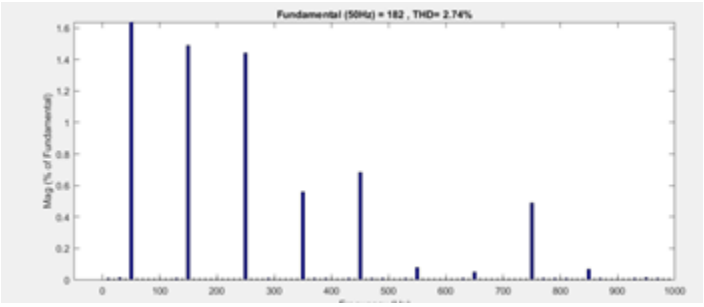

Fig 7: Harmonic profile of the proposed MLI

6 CONCLUSION

Modern days MLI topologies have been more popular in renewable energy applications. The proposed multilevel inverter has many advantages such as a smaller number of switches, drive circuits, and the DC Source count. Compared to the conventional MLI topologies minimum number of conducting switches is required to generate the higher voltage level. Therefore, the switching losses and conducting losses are considerably low. The proposed topology tested with MATLAB/SIMULINK environment. As a result, the proposed configuration produces high voltage with a lesser number of components and a lower percentage of THD and it is well suitable for Photovoltaic applications and any renewable energy resources.

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