A Low NF, High Gain Of 2.4ghz Differential LNA Design For Wireless Applications

Mahesh Mudavath, K. Hari Kishore

Abstract: This article presents the differential Low Noise Amplifier (LNA) for wireless receiver at the frequency of 2.4GHz. This differential LNA provides less noise figure (NF), high gain and good reverse isolation as well as good stability. The designed LNA is simulated with a 180 nanometers CMOS process in cadence virtuoso tool and simulate the results by using SpectreRF simulator. This LNA exhibits an input reflection coefficient (S_{11}) of -8.4dB and output reflection coefficient (S_{22}) of -10dB. It produces a noise figure (NF) of 0.54dB, a high voltage gain (S_{21}) of 30dB, a good reverse isolation (S_{12}) of -48dB, and it maintains good stability of Rollet factor $K_f > 1$, and also alternate stability factor $B_{1f} < 1$, respectively.

Index Terms: Cascode-stage; cascade differential; input matching; inductive source degeneration; low noise amplifier; noise figure.

1. INTRODUCTION

In modern years, an instantaneous improvement in technology as well as market has raised better quality by means of telecommunications and portable electronic devices [1]. The majority of the communication systems could be hand-held; hence device with compressed size is a challenging task for IC manufacturer. The key challenge for compact device size of such systems, directly that it affects power usage and portability. Conversely, the essential demands of high frequency devices for huge data rate wireless systems such as IoT (internet of things) [2], and wireless LAN. These are broadly used in homes and offices to offer multi-standard receivers [3]. By 2020 the number of IoT portable devices will go beyond 40 billion and more and it will be used at extremely wide area such as an urban area, an indoor area, a mountain area and so forth [2]. CMOS technology for high frequency integrated circuits is an appropriate solution. In an advanced CMOS process the challenging factors for design and development of the LNA building blocks are circuit linearity, decreasing supply voltage, low noise figure (NF), and high gain. The receivers are broadly utilized in RF radio frequency systems. In reality, a receiver is capable to accept every signal from low to high frequency, and the received signals are typically very noisy and weak [1]. Consequently, the LNA is desired to amplify the received signals and transfer to the subsequent stages. Annually, there are many techniques have been exploring for LNA design. Nonetheless, all design parameters simultaneously can't be satisfied or achieved for a Radio Frequency (RF) system. Hence, a trade-off between the issues of LNA is supposed to be done as to achieve an adequate performance over the preferred bandwidth. For the design of LNA, noise figure is one of the important key parameter, as it shows the entire system noise presentation in a receiver, and also more power gain, low power consumption, and good input matching are significant key parameters [1].

Here, the simple way to design a cascade-stage and differential LNA to amplify weak and noisy signals for wireless receivers [4]. However, this approach requires increases the complication of the receiver, and bulky chip area [3]. The substitute technique employs the switched inductors, or switched capacitors, in the input and output matching networks. This switching technique can't offer an appropriate match for both band of frequency and it also restrictions to receive one frequency band at a time. But the cascade differential LNA design is able to offer an improved trade-off between power gain, & noise figure [3]. This paper is prearranged as follows. Section-2 covers the importance of low noise amplifier and different blocks. Section-3 explains the different techniques of LNA topologies and fundamental theoretical calculations for design parameters. Section-4 is the description about the circuit design and analysis. The simulation plots are exposed in Section-5 and finally, Section-6 concludes this paper.

- *Research Scholar, KLEF (Deemed to be University), Vaddeswaram, Guntur Dist. (AP), India.*
- *Asst. Professor, Vaagdevi College of Engineering. Bollikunta, Warangal (TS), India. mahichauhan@gmail.com*
- *KLEF (Deemed to be University), Vaddeswaram, Guntur (AP), India*
- *Kakarla.harikishore@kluniversity.in*

2. LOW-NOISE AMPLIFIER

Every signal is analog and we handle with the right device & flow. A low-noise amplifier is the foremost stage of the receiver front-end and it is used to amplify the signal which is coming from the antenna terminals whilst introducing a smaller amount of noise by the same LNA [5]. Actually the LNA consist of five different parts, which are appropriate topologies, input impedance matching network, inductive source degeneration circuit, biasing circuit, and output impedance matching network. The universal topology of any LNA circuit can be consists of three stages. It has the input matching block, core amplifier and finally output matching block. To get better design performance the input/output matching network can try to maintain similarity. It is measured from s-parameters of input return loss co-efficient S_{11} and output return loss co-efficient S_{22}. Generally, these values should be in the range of less than or equal to -10dBm.

The stability of the two-port network is analyzed using s-parameters. The essential and sufficient condition for stability is to take Rollet factor $K_f > 1$ and also alternate stability factor $B_{1f} < 1$, which are expressed in terms of s-parameters [1].

$$K_f = \frac{(1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2)}{(2\,|S_{12}*S_{21}|)} \quad (1)$$

$$|B_{1f}| = 1 + |S_{11}|^2 - |S_{22}|^2 - \Delta \quad (2)$$

Where

$$\Delta = (S_{11}.S_{22} - S_{12}.S_{21})$$

If $K_f > 1$ & $B_{1f} < 1$, the network would be unconditionally stable.

3. SINGLE-ENDED, CASCODE STAGE, AND CASCADE DIFFERENTIAL AMPLIFIER

The amplification block of the cascode circuit is revised during this analysis to attain an optimized performance in single-ended and differential topologies. A single-ended signal measured with relation to a preset potential-gnd. Further, as a result of the differential signal measured between each node that have equivalent and opposite excursions in the order of a fixed potential. To be precise each node should exhibit equivalent impedances to its potential. The center potential within the differential signal is named the common-mode level.

3.1. Single transistor amplifier

An amplifier may be a device for increasing the ability of a signal. This can be often accomplished by taking power from V_{dd} and controlling the output to duplicate the form of the V_i signal but with a bigger (current or voltage) amplitude. During this sense, an amplifier could be attention of as modulating the voltage or current of the ability of a signal to provide its output.

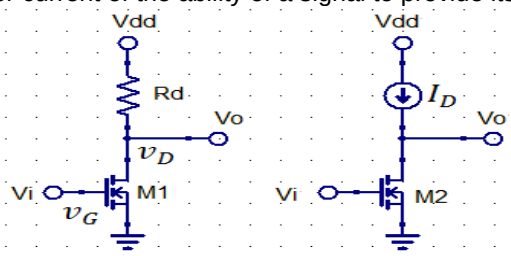

***Fig. 1**. Single transistor amplifier*

To measure the drain current I_D, shown in Fig. 1 it is a function of gate voltage v_G which is applied at the gate terminal, and drain voltage v_D which is taken from the drain terminal.

$$I_D = f(v_G, v_D) \quad (3)$$

For multiple signals, by applying partial derivation to the equation 3, then the change of current I_D defined as.

$$\partial I_D = \frac{\partial I_D}{\partial v_G}.\partial v_G + \frac{\partial I_D}{\partial v_D}.\partial v_D \quad (4)$$

Since

$$\frac{\partial I_D}{\partial v_G} = g_m$$

and

$$\frac{\partial I_D}{\partial v_D} = g_o$$

Assumed $\partial v_G = v_i$ and $\partial v_D = v_o$ then

$$\partial I_D = g_m v_i + g_o v_o$$

$0 = g_m v_i + g_o v_o$ (Suppose ∂I_D is very small)

Then the voltage gain A_V can be defined as

$$A_V = \frac{v_o}{v_i} = -\frac{g_m}{g_o} = -g_m r_o \quad (5)$$

Assuming transistor M_1 is in saturation region, and then the I_D current can be expressed as.

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)[v_{Gs} - v_{th}]^2 \text{ -------For saturation region}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left[(v_{Gs} - v_{th})v_{Ds} - \frac{1}{2}v_{Ds}^2\right] \text{ ---For linear region}$$

For MOSFET should have I_D varied to the signal applied at input. In saturation region, I_D varies with respect to input voltage else I_D varies both v_{Gs}, and v_{Ds} .

$$v_{th} = v_{T0} + (\alpha - 1)v_s$$

Define

$$v_{th} = v_G - v_{T0} - \alpha v_s$$

And

$$v_{GS} = v_G - v_s$$

$$I_D = \frac{K}{2\alpha}{v_{GT}}^2$$

Where $K = \mu_n C_{ox}\left(\frac{W}{L}\right)$

$$g_m = \frac{\partial I_D}{\partial v_G} = \frac{K}{\alpha}v_{GT}$$

$$v_{GT} = \sqrt{\frac{2\alpha I_D}{K}}$$

$$g_m = \frac{K}{\alpha}\sqrt{\frac{2\alpha I_D}{K}} = \sqrt{\frac{2KI_D}{\alpha}} \quad (6)$$

$$g_m = \frac{2I_D}{{v_{GT}}^2}v_{GT}$$

3.2. Cascode transistor amplifier

The signal flows through the gate of the first transistor M_1, and the gate of the second transistor M_2. The bias reference voltage V_{ref} is fixed at gate of the second transistor M_2, such that both transistors operate in saturation mode. The lower transistor acts as a common source amplifier, whereas the upper transistor works in the common gate configuration and also it act as isolating output nodes from input.

To analyze the cascade stage and its circuit performance, we treat the two series connected transistors as a single compound transistor with the gate and source of M_1 and drain of M_2 acting as the corresponding terminals of the equivalent transistor.

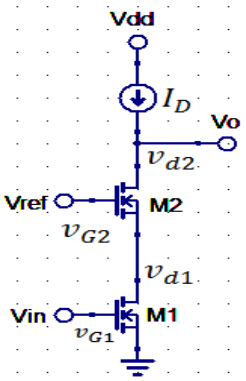

***Fig. 2**. cascode amplifier*

To measure the drain current I_D for cascode amplifier shown in Fig. 2 is a function of gate voltage v_G which is applied at the gate terminal, and drain voltage v_D which is taken from output of drain terminal.

$$I_D = f(v_G, v_D)$$

$$\partial I_D = g_{meq}\partial v_{G1} + g_{oeq}\partial v_{D2}$$

$$g_{meq} = \left.\frac{\partial I_D}{\partial v_{G1}}\right|_{\partial v_{D2}=0}$$

$$g_{oeq} = \left.\frac{\partial I_D}{\partial v_{D2}}\right|_{\partial v_{G1}=0}$$

$$\partial v_{Ds2} = \partial v_{D2} - \partial v_{S2} = 0 - \partial v_{S2} = -\partial v_{d1}$$

$$\partial v_{Gs2} = \partial v_{G2} - \partial v_{S2} = 0 - \partial v_{S2} = -\partial v_{d1}$$

We then evaluate its equivalent g_{meq} and g_{oeq}. Since the two transistors are in series, then the drain currents of both transistors are equal i.e.

Here, current for both M_1 and M_2

$$I_{D1} = g_{m1}v_{G1} + g_{o1}\partial v_{D1}$$

$$I_{D2} = -g_{m2}v_{D1} - g_{o2}v_{D1}$$

$$where\ I_{D1} = I_{D2} = I_D$$

$$v_{D1} = -\frac{I_D}{g_{m2} + g_{o2}}$$

$$I_D = g_{m1}v_{G1} - I_D\frac{g_{o1}}{g_{m2} + g_{o2}}$$

$$I_D\left[1 + \frac{g_{o1}}{g_{m2} + g_{o2}}\right] = g_{m1}v_{G1}$$

$$g_{meq} = \frac{I_D}{v_{G1}} = g_{m1}\frac{1}{\left[1 + \frac{g_{o1}}{g_{m2} + g_{o2}}\right]}$$

$$g_{m2} >> g_{o2}$$

Generally g_m values are very much higher than g_o values. In this case, we can see that

$$g_{meq} \cong g_{m1}$$

$$g_{oeq} = \frac{\partial I_D}{\partial v_{D2}}\Big|_{\partial v_{G1}=0}$$

We should make $\partial v_{G1} = 0$ and evaluate the change of drain current I_D according with change in the drain voltage of M_2 to get g_{oeq}.

$$\partial v_{gs1} = 0$$

$$\partial v_{gs2} = \partial v_{G2} - \partial v_{s2} = -\partial v_{d1}$$

$$\partial v_{ds2} = \partial v_{d2} - \partial v_{d1}$$

$$I_d = 0 + g_{o1}v_{d1} \quad \text{(for } M_1\text{)}$$

$$I_d = -g_{m2}v_{d1} + g_{o2}(v_{d2} - v_{d1}) \quad \text{(for } M_2\text{)}$$

$$v_{d1} = \frac{I_d}{g_{o1}}$$

$$I_d = -I_d\frac{g_{m2} + g_{o2}}{g_{o1}} + g_{o2}v_{d2}$$

$$g_{oeq} = \frac{I_D}{v_{D2}} = \frac{g_{o1}g_{o2}}{g_{o1} + g_{o2} + g_{m2}}$$

But $r_{oeq} = \frac{1}{g_{oeq}}$

$$g_{m2} >> g_{o1} \text{ and } g_{o2}$$

$$g_{oeq} = \frac{g_{o1}g_{o2}}{g_{m2}}$$

$$r_{oeq} = g_{m2}.r_{o2}.r_{o1}$$

We can define the individual DC gains of the two transistors (in CS and CG configurations respectively) [6]. Then the voltage gain A_V can be defined as.

$$A_o = -\frac{g_{meq}}{g_{oeq}} = -\frac{g_{m1}(g_{m2}+g_{o2})}{g_{o1}+g_{o2}+g_{m2}} \times \frac{g_{o1}+g_{o2}+g_{m2}}{g_{o1}g_{o2}}$$

$$A_o = -\frac{g_{m1}(g_{m2} + g_{o2})}{g_{o1}g_{o2}}$$

$$A_o = -\frac{g_{m1}}{g_{o1}}\left[1 + \frac{g_{m2}}{g_{o2}}\right]$$

$$A_{o1} = -\frac{g_{m1}}{g_{o1}} \quad \text{------- For CS stage}$$

and

$$A_{o2} = \left[1 + \frac{g_{m2}}{g_{o2}}\right] \quad \text{---- For CG stage}$$

$$A_o = A_{o1}.A_{o2} \qquad (7)$$

Here, the effective g_m of cscode is same as the single transistor amplifier.

3.2.1. AC behavior

The small- signal model analysis for cascode transistor shown in Fig. 3. The equivalent transconductance g_{meq} for the cascode stage is regarding the similar to the single transistor stage, the product of Gain Bandwidth $(G \times B)$ also remains unchanged. Because of high output impedance, the bandwidth is reduced and the DC gain is increased for a cascade-stage.

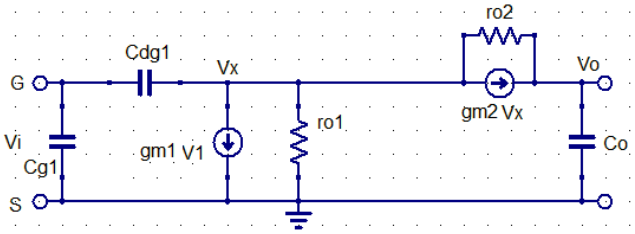

Fig. 3*. The small- signal model analysis for cascode.*

Writing the KCL equation at the output we get

$$g_{m2}v_x + \frac{v_x - v_o}{r_{o2}} = sC_o v_o$$

This leads to

$$v_x(1 + g_{m2}r_{o2}) = (1 + sC_o r_{o2})v_o$$

$$v_x = \frac{1 + s\,C_o r_{o2}}{1 + g_{m2}r_{o2}}v_o = \frac{1 + s\,C_o r_{o2}}{A_2}v_o$$

Since A_2 is quite large, v_x is very small compare to v_o, KCL at the drain of the lower transistor is.

$$sC_{dg1}(v_i - v_x) = g_{m1}v_i + \frac{v_x}{r_{o1}} + sC_o v_o$$

$$\left(sC_{dg1}v_i - sC_{dg1}v_x\right) = \frac{g_{m1}r_{o1}v_i + v_x + sC_o r_{o1}v_o}{r_{o1}}$$

$$\left(sC_{dg1}v_i - sC_{dg1}v_x\right)r_{o1} = g_{m1}r_{o1}v_i + v_x + sC_o r_{o1}v_o$$

$$v_i\left(sC_{dg1}r_{o1} - g_{m1}r_{o1}\right) = v_x\left(1 + sC_{dg1}r_{o1}\right) + sC_o r_{o1}v_o$$

$$v_i\left(sC_{dg1}r_{o1} - g_{m1}r_{o1}\right) = \frac{1 + s\,C_o r_{o2}}{A_2}v_o\left(1 + sC_{dg1}r_{o1}\right) + sC_o r_{o1}v_o$$

$$v_i\left(sC_{dg1}r_{o1} - g_{m1}r_{o1}\right) = v_o\left[\frac{(1 + s\,C_o r_{o2})\left(1 + sC_{dg1}r_{o1}\right)}{A_2}\right] + sC_o r_{o1}v_o$$

$$v_i\left(sC_{dg1}r_{o1} - g_{m1}r_{o1}\right) = v_o\left[\frac{(1 + s\,C_o r_{o2})\left(1 + sC_{dg1}r_{o1}\right) + A_2 sC_o r_{o1}v_o}{A_2}\right]$$

This gives

$$\frac{v_o}{v_i} = \frac{\left(sC_{dg1}r_{o1} - g_{m1}r_{o1}\right)A_2}{(1 + s\,C_o r_{o2})\left(1 + sC_{dg}r_{o1}\right) + A_2 sC_o r_{o1}}$$

$$\frac{v_o}{v_i} = -\frac{\left(A_1 - sC_{dg}r_{o1}\right)A_2}{(1 + s\,C_o r_{o2})\left(1 + sC_{dg}r_{o1}\right) + A_2 sC_o r_{o1}}$$

If $sr_{o1}C_{dg}$ is small we can simplify the above relation to get.

$$Voltage\ gain(A_v) = \frac{v_o}{v_i} = -\frac{A_1 A_2}{1 + s\,C_o r_{o1}\left(A_2 + \frac{r_{o2}}{r_{o1}}\right)} \qquad (8)$$

3.3. Differential amplifier

The differential of LNA is broadly used because of its advantages of common-mode (CM) noise immunity [7]. Hence, they offer differential output that is needed by the following stages of LNA shown in Fig. 4. The selection of cascode topology within initial stage degrades the noise presentation of the amplifier yet if it improves the gain. To occupied less chip area by using single ended LNAs, but if the amplifier design is single ended, it's a lot of vulnerable to noise and alternate interferences [8].

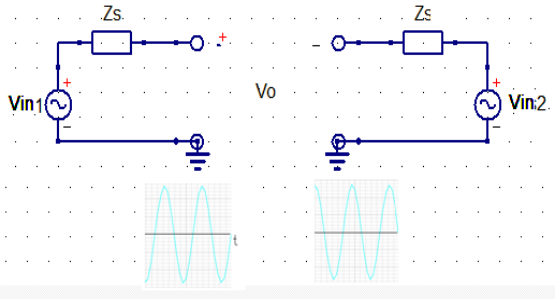

Fig. 4. *Differential outputs.*

Alternatively, by using the differential amplifier very less amount of liable to noise and intervention are presented [9]. Also the differential amplifier has the advantage, of getting the signal swing which will be a double that of the single-ended swing lying on the similar supply voltage, in that way increasing signal-to-noise ratio (SNR) [8].

3.3.1. Noisy supply voltages

For single ended operation, if V_{dd} changes by ΔV, then output also changes by the same amount shown in Fig 5.

- Output is quite susceptible to supply noise.
- Differential operation: if the circuit is symmetric, supply noise affects V_x and V_y but not $V_x - V_y$ [10] .

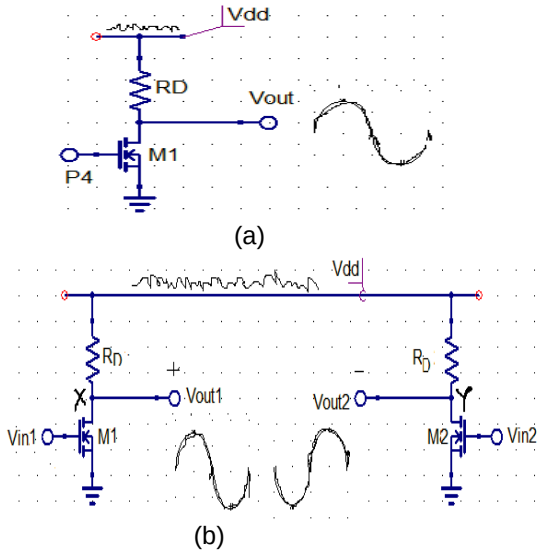

Fig. 5*. Noisy signals for (a) single-ended (b) differential paths*

Max achievable voltage swings increase.
Max output swing at X or Y is $V_{dd} - (V_{GS} - V_{TH})$
Where as $V_X - V_Y$ is $2[V_{dd} - (V_{GS} - V_{TH})]$
Simpler biasing and higher linearity
Disadvantages:
Double the area with respect to single ended counterpart
Advantages of differential signaling

1. Employing differential paths for sensitive signals, higher immunity to environmental noise
2. Noise cancelled.
3. Highest achievable voltage swings
4. Simpler biasing and better linearity

Conclusion: Because of symmetry, common mode signal rejected.

3.4. INPUT MATCHING AND GAIN

The most important purpose of input matching n/w is to attain the maximum power transfer rate from input to output terminals, which is happens when impedance matches. The received signals from the antenna terminals, assumed as voltage source V_s that is connected to a LNA. The source impedance (Z_s), generally the resistance of the antenna's, can be specified as 50Ω. For that reason, the LNA's input impedance (Z_{in}), be required to match the exact 50Ω in regulate to transfer the maximum power to the subsequent stage of the system [11].

The input impedance of designing LNA can be expressed as beneath equation (9) [8] [12].

$$Z_{in} = jw(L_g + L_s) + \frac{1}{jw(C_{gs}+C_{ex})} + \frac{g_m}{(C_{gs}+C_{ex})}L_s \qquad (9)$$

Where, g_m & C_{gs} are the transconductance and gate-source capacitor of the M_1 respectively. The input impedance matching network consists of, L_g, L_s and C_{ex} resonate at the frequency of operation, the imaginary part of impedance Z_{in} is neglected [13]. For this context, the pure real part will be considered for input impedance with only relevant to L_s & C_{ex}, consequently by adjusting L_s & C_{ex} can simply realize to a real 50Ω impedance at the input of the LNA can be expressed as below equation(10) [14].

$$Z_{in} = \frac{g_m}{(C_{gs}+C_{ex})}L_s = 50\Omega \qquad (10)$$

To calculate the required Z_{in} of LNA with the help of L_g, L_s, g_m, C_{ex}, and C_{gs}.
As a result, L_g and L_s can be obtained by equation 11 and 12 [15].

$$L_g = \frac{1}{\omega_0^2 C_{gs} C_{ex}} - L_s \qquad (11)$$

$$L_s = Z_{in}\frac{(C_{gs}+C_{ex})}{g_m} \qquad (12)$$

Hence, the voltage gain A_v can be defined as.

$$Voltage\ gain(A_v) = \frac{v_o}{v_i} = -\frac{A_1 A_2}{1+s\,C_o r_{o1}\left(A_2+\frac{r_{o2}}{r_{o1}}\right)} \qquad (13)$$

4. CIRCUIT DESCRIPTION

A. Cascode Configuration.

The universal topology of LNA is consists of 3 stages: staring with input matching set-up, the core amplifier design, and finally the output matching set-up [16]. To begin with, input matching necessities are fulfilled by putting an inductor L_g at gate of MOSFET transistor it allows resonating at the centre freq. To realize low NF in given structure, an inductor L_s is located on source terminal; it acts as inductive source degeneration [16]. The capacitance C_{gd} is worn for wide-band matching. Therefore the L_g, C_{gd} and L_s provide the input matching network for wide-band matching. At the output side L_d and C_d is resonating to a particular frequency [16].

B. Cascade Differential Configuration

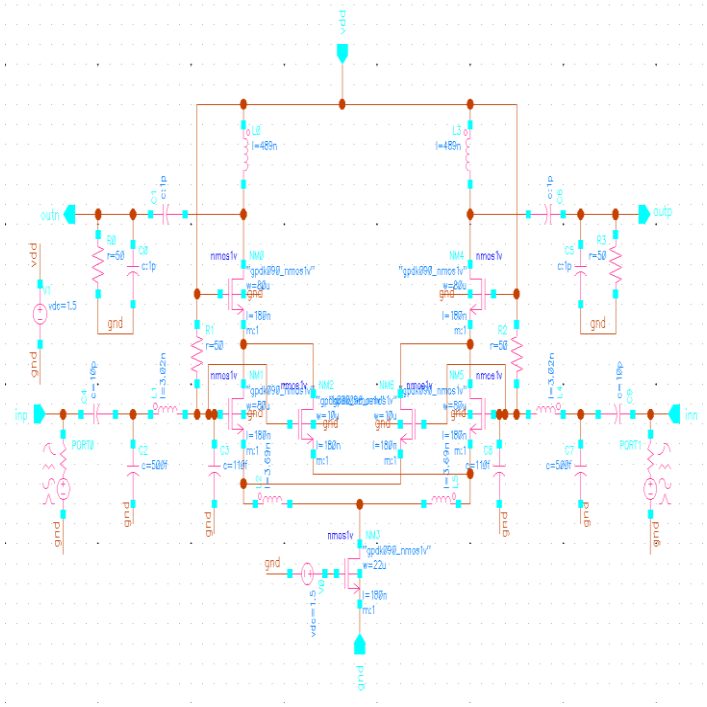

***Fig. 6**. Differential circuit design*

The projected differential cascade LNA [17] [18] is illustrates in Fig. 6. This differential design includes the each side inductive degenerated CS and a CG stage of transistor M_1 and M_2. Also it consists of input gate inductor L_g, source inductor L_s, gate-to-source capacitors C_{gs}, respectively for both sides [17]. The benefit of input output and noise matching simultaneously, with the help of inductive source degenerated through inductor L_s. For the purpose of input matching at the input ports, the DC blocking capacitor C_B and an off chip capacitor C_p are used. To optimize the power gain & noise of the LNA, a very small value of shunt capacitance C_s is connected at the input port. Transistors M_5 and M_6 commonly called as cascade devices, hence it formed as CG stage cascaded to the input stage [17] [19]. The benefit of the cascade device using in LNA circuit is essentially shields the output from the input stage; hence it extremely improves the power gain and reverse isolation (S_{12}) [20]. At the output ports, the LC resonance tank circuit consists of the MIM capacitors C_1, C_2, tuning inductor L_T, and the total drain terminal to node capacitances are required to tuning the desired frequency and also for output impedance matching.

5. SIMMULATED RESULTS

The design parameters of the LNA circuit are analyzed with respect to the frequency of 2.4GHz operation. A plot of the S-parameters and required parameters is shown from Fig. 7 to Fig. 13. The S_{21} plot is of importance as it gives the gain of the amplifier. As it can be seen from Fig. 7, a gain of 30dB is obtained at 2.4GHz which falls right in our desired range.

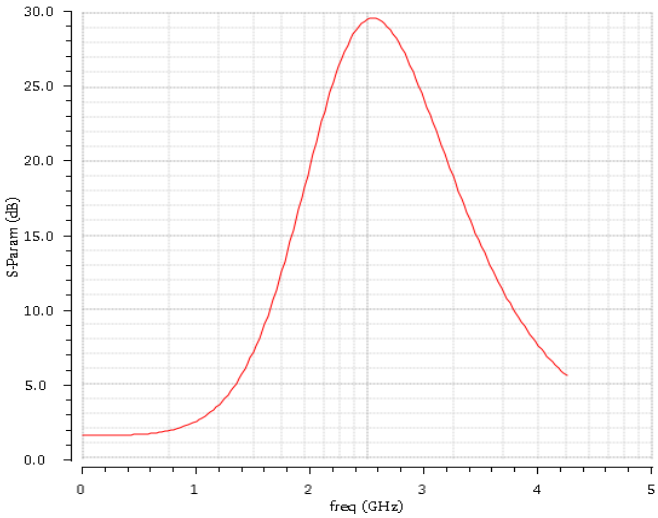

***Fig. 7** Simulated voltage gain S_{21}=30dB @ 2.4GHz center frequency*

The plot of Noise Figure is shown in the Fig. 8, a noise figure (NF) of 0.54dB @ 2.4GHz is obtained.

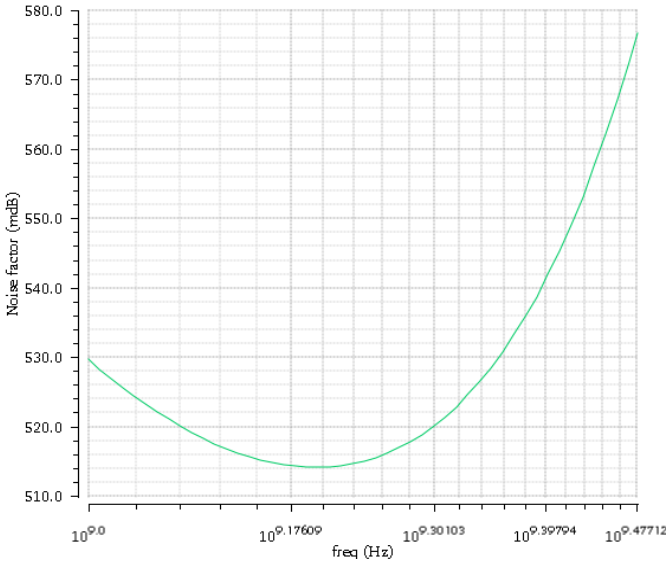

***Fig. 8** Simulated noise figure (NF) =0.54dB @ 2.4GHz center frequency*

Fig. 9 gives the plot of the reverse isolation (S_{12}) that is provided by the circuit. The value of the isolation that was obtained is -48dB @ 2.4GHz which are very good figure. This is attributed to the resonating circuit that is inserted between the two stages.

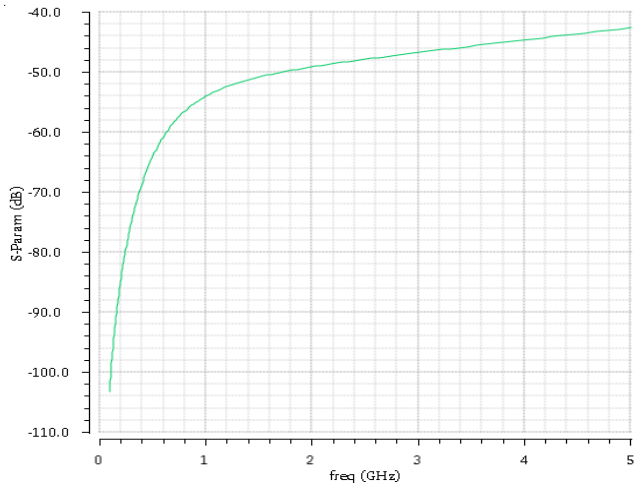

Fig. 9 *Simulated reverse isolation (S_{12}) = -48dB @2.4GHz center Frequency*

Fig. 10 shows the plot of the input reflection coefficients (S_{11}), and its obtained value is -8.4dB @ 2.4GHz

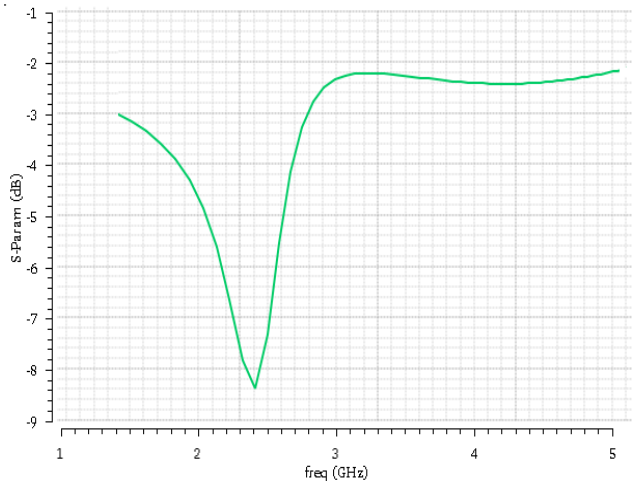

Fig. 10 *Simulated input return loss S_{11}= -8.4dB @ 2.4GHz center frequency*

Fig. 11 shows the plot of the output reflection coefficients (S_{22}), and its obtained value is -10dB @ 2.4GHz.

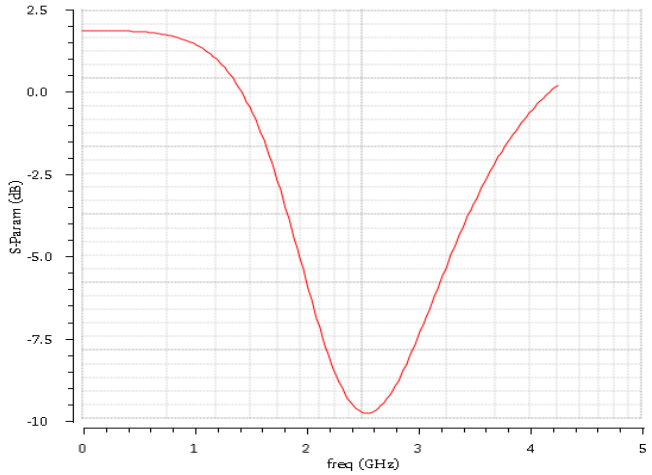

Fig. 11 *Simulated output return loss S_{22}= -10dB @ 2.4GHz center frequency*

Fig. 12 presents P_{1dB} compression point which is -10.6dBm and linearity performance of the proposed LNA.

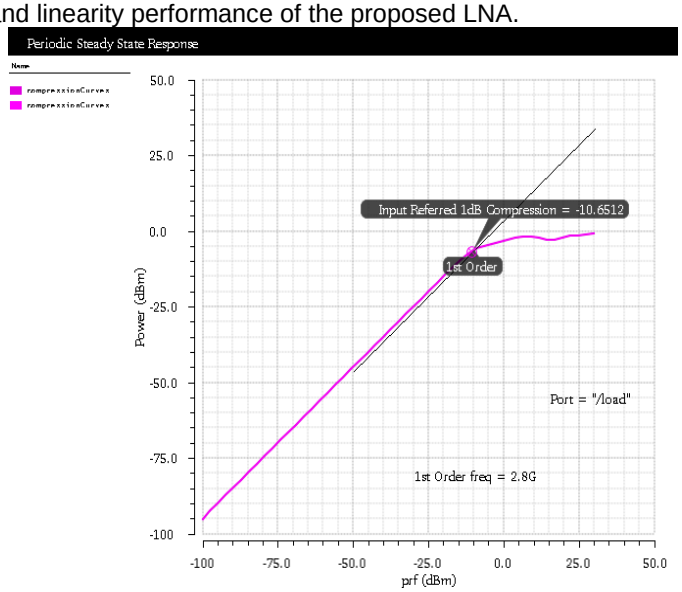

Fig. 12 *The simulated 1dB Compression point (P_{1dB}) =-10.6dBm*

IIP_3 of the designed LNA is presented in Fig. 13, with respect to this figure, its value is -14dBm.

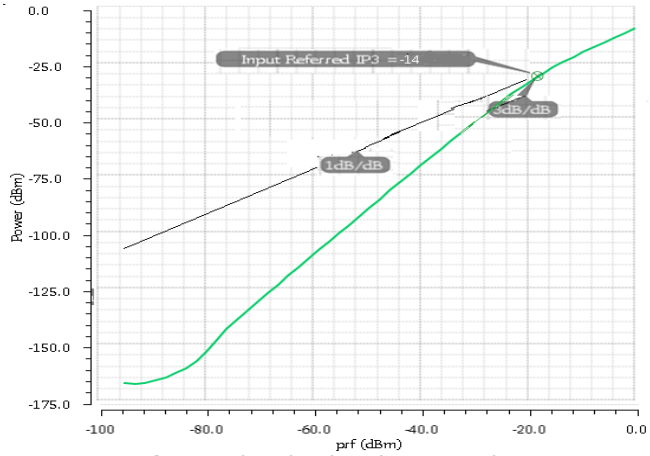

Fig. 13 *The simulated IIP_3=-14dBm*

The simulated results are summarized and compared to other related works in the area of LNA design and also with some designs employing the cascode and cascade strategy. The results are tabulated in table 1.

Table 1: *Performance summary and comparison of CMOS LNAs*

Parameters	This work	[9]	[2]		[4]	
Center Frequency (GHz)	2.4	2.4	2.4	5.2	1.2	1.57
CMOS Tech. (nm)	180	180	180		180	
Power Gain (dB)	30	12.68	16.5	11.1	26.9	27.5
Noise Figure (dB)	0.54	3.14	3.1	3.7	2.3	2.3
S_{11} (dB)	-8.4	-13.5	-14	-16	-11	-13
S_{12} (dB)	-48	-33.8	--			
S_{21} (dB)	30	12.68	16	11	26.9	27.5

S_{22}	-10	-10	-6	-8		
1dB Compression point (P_{1dB})	-10.6					
IIP_3(dB)	-14					
Stability Factor (K_f) (B_{1f})	1.09 0.97	4.84 0.94	10	5	--	--
Power supply (V)	1.8	1.8	1.8		1.8	

6. CONCLUSION:

The field of wireless receiver communications has undergone enormous growth, moving quickly during a sequence of generations in the present scenario. The receiver design with low noise is a foremost design constraint. For this context, the design of the LNA for better performance is of immense importance. The proposed LNA for Radiofrequency front-end is designed with very little NF & high gain using 180nanometer in cadence virtuoso tool and simulate the results by using SpectreRF simulator. This LNA exhibits an input reflection coefficient (S_{11}) of -8.4dB and output reflection coefficient (S_{22}) of -10dB. It produces a noise figure (NF) of 0.54dB, a high voltage gain (S_{21}) of 30dB, a good reverse isolation (S_{12}) of -48dB, and it maintains good stability of Rollet factor $K_f > 1$, and also alternate stability factor $B_{1f} < 1$, respectively.

REFERENCES:

[1] Tayebe Mohammadi, Alireza Ghaneizadeh, and and Yasser Mafinejad, "A Narrow-Band CMOS LNA for Wireless Communications," in 26th Iranian Conference on Electrical Engineering (ICEE2018), 2018, pp. 265-268.

[2] Atsuhiro Hamasawa and Haruichi Kanaya, "Dual-band differential outputs CMOS Low Noise Amplifier," in 2018 IEEE 20th Electronics Packaging Technology Conference (EPTC), Singapore, pp. 661-664.

[3] Hossein Khosravi, Salman Zandian, Abolfazl Bijari, and Nabeeh Kandalaft, "A Low Power, High Gain 2.4/5.2 GHz Concurrent Dual-Band Low Noise Amplifier," in 2018 IEEE 9th Annual Computing and Communication Workshop and Conference (CCWC), Las Vegas, NV, USA, 2018, pp. 0788-0792.

[4] M. Safari, M. Eghtesadi, and M. R. Mosavi, "A Concurrent Dual-Band Low Noise Amplifier for GNSS Receivers," Iranian Journal of Electrical and Electronic Engineering, vol. 12, no. 2, pp. 119-125, June 2016.

[5] M.Sumathi and S.Malarvizhi, "Study on Performance Analysis of CMOS RF front-end circuits for 2.4GHz Wireless Applications," Study on Performance Analysis of CMOS RF front-end circuits for 2.4GHz Wireless Applications International Journal of Electrical and Electronics Engineering (IJEEE), vol. I, no. II, pp. 18-23, 2011.

[6] Pratap Tumkur Renukaswamy, Vijaya Pasupureddi, and and Johannes Sturm, "Analysis and Design of Differential Feedback CG LNA Topologies for Low Voltage Multistandard Wireless Receivers," in 2016 24th Austrian Workshop on Microelectronics, 2016, pp. 24-29.

[7] Ratan Smrity et al., "Design of 2.4 GHz Differential Low Noise Amplifier Using 0.18µm CMOS Technology," in International Conference on Computing, Communication, and Automation, 2016, pp. 1435-1439.

[8] Raghu S and Punithavathi Duraiswamy, "High Gain and Low Noise Figure Single-to-Differential CMOS LNA for Ka-Band Communication System," in IEEE MTT-S International Microwave and RF Conference (IMaRC), 2017 , pp. 35-38.

[9] Nandini Shrivastava and Rajesh Khatri, "Design of a 2.4-GHz Differential Low Noise Amplifier using 180nm technology," in Proceeding International conference on Recent Innovations is Signal Processing and Embedded Systems (RISE-2017), 2017, pp. 494-497.

[10] Dhananjaya Tripathy, Shasanka Sekhar Rout, and Kabiraj Sethi, "A Low Power Noise Cancelling LNA for UWB Receiver Front End," in 2015 IEEE Power, Communication and Information Technology Conference (PCITC), Bhubaneswar, India., 2015.

[11] Mahesh Mudavath and K. Hari Kishore, "Design and Analysis of Receiver Front-End of CMOS Cascode Common Source Stage with Inductive Degeneration Low Noise Amplifier on 65 nm Technology Process," Journal of Computational and Theoretical Nanoscience, vol. 16, no. 5-6, pp. 2628-2634, May 2018.

[12] Mahesh Mudavath and K.HariKishore, "Design of CMOS RF Front-End of Low Noise Amplifier for LTE System Applications," Asian Journal of Information Technology, Medwell Journal, vol. 15, no. 20, pp. 4040-4047, 2016.

[13] A. Surendar, K. H. Kishore, M. Kavitha, A. Z. Ibatova, V. Samavatian "Effects of Thermo-Mechanical Fatigue and Low Cycle Fatigue Interaction on Performance of Solder Joints," IEEE Transactions on Device and Materials Reliability, P-ISSN: 1530-4388, E-ISSN: 1558-2574, Vol No: 18, Issue No: 4, Page No: 606-612, December-2018.

[14] Mahesh Mudavath and K Hari Kishore, "RF Front-End Design of Inductorless CMOS LNA Circuit with Noise Cancellation Method for IoT Applications," International Journal of Innovative Technology and Exploring Engineering (IJITEE), vol. 8, no. 6S, pp. 176-183, April 2018.

[15] Vaithianathan, J. Raja, R. Kavya, and N. Anuradha, "A 3.1 to 4.85GHz differential CMOS low noise amplifier for lower band of UWB applications," in 2010 International Conference on Wireless Communication and Sensor Computing (ICWCSC), Chennai, India, 2010.

[16] J.Manjula, P.Sai Krishna, and and D.Rubeena, "Design and Performance Analysis of Active Inductor Based Reconfigurable Regulated Cascode LNA for Tunable RF Front End," in International Conference on Communication and Signal Processing, India, April 6-8, 2017, pp. 0222-0227.

[17] Shaikh K. Alam and Joanne DeGroat, "A 1.5-V 2.4 GHz Differential CMOS Low Noise Amplifier for Bluetooth and Wireless LAN Applications," in 2006 IEEE North-East Workshop on Circuits and Systems, Gatineau, Que., Canada, 2006, pp. 13-16.

[18] Jinhua Liu, Guican Chen, and Ruizhi Zhang, "Design of a noise-canceling differential CMOS LNA for 3.1–10.6 GHz UWB receivers," in 2009 IEEE 8th International Conference on ASIC, Changsha, Hunan, China, 2009, pp. 1169-1172.

[19] Neeraja A R and Siva S Yellampalli, "Design of Cascaded Narrow Band Low NoiseAmplifier," in 2017 International Conference on Electrical, Electronics, Communication, Computer and Optimization Techniques (ICEECCOT).

[20] Shaikh K. Alam and and Joanne DeGroat, "A 1.5-V 2.4 GHz Differential CMOS Low Noise Amplifier for Bluetooth and Wireless LAN Applications," in 2006 IEEE North-East Workshop on Circuits and Systems, 2006, pp. 13-16.