Performance Analysis Of Analog Data Compression And Decompression Using ANN In 32nm Finfet Technology

Sujata.A.A and Dr. Lalitha.Y.S

Abstract: The extension within the production of IC for applications of VLSI domains like medicine imaging, Signal processing and telecommunication are becomes a desire for brand spanking new technologies and existence. These productions are due to the approach of advantages of VLSI technology. The additional varieties of researchers are operating for medicines Sciences to create things are less complicated and robotic. Absolutely genetic performances abundant nearer to artificial Neural Network (ANN) are generally used for information compression and reconstruction of medical field signal, organizations and identification of diseases. For signal compression and reconstruction using PCA, HMM and DCT techniques are generally used, however losses are a lot of. To deal with these problems, the chip level style exploits FinFET 32 nm technology for ANN is projected and it consists of Gilbert cell number, sigmoid activation function (SAF) and bias circuits that are supports to extend the compact magnitude relation and precision. In view of this paper, ANN has been outlined in Cadence Virtuoso analog tool employing FinFET 32nm technology, all sub-units are outlined from Layout level to design through LVS, DRC and RC Extraction, and eventually chip level i.e. GDS-II level. ANN predominantly aims at the style of Feed Forward Artificial Neural Network (FWANN) and it's instructed by employing Back Propagation (BP) design. The overhaul loads hold on 16bit 6T SRAM cell, the counterfeit results has been created 10% increase in delay, 7.5% improvement in power consumption and 0.5% information loses compressed subsequently.

Index Terms: ANN, Data Compression and Decompression, FinFET, 32um Technology, Multiplier, VLSI.

1 INTRODUCTION

Robust system is flexible in such a way that its performance enhance through communication with its atmosphere. Present applications for robust systems are in fields such as transmissions, Direction finding, geophysics, navigation systems, and medicine natural philosophy. The crucial and fundamental property of the robust system is its time-fluctuations, self-modifying factor. The adaptive system is commonly nonlinear in its quality. However intelligence could be a biological word and is non-heritable from experiences. Therefore science that deals with perception mathematically is named as Artificial Intelligence (AI).

2 DESIGN METHODOLOGY FOR NEURAL NETWORK WITH ADAPTIVE FILTERING

In this work, there are four pulses having different pulse widths as input data to ANN and same data is processed through Gilbert cell multiplier, single neuron and activation function for compression of the data into single data as shown in Fig.12. The compressed single data is input to the decompression for reconstruction of the original data as shown in Fig.15. The proposed model network consists of input, output, and hidden layers along with signals. There are many sorts of adjustable filtering for neural network applications that we've considered: one is Network modeling: In several applications, a network of concealed fabric has noticeable input, and output signals. A way of getting information concerning the concealed system's effective model is to use its input to associate applicable neural network and to utilize its output because the target worth of the neural network. The neural network develops a feedback to match that of the concealed network. The network modeling and its performance employing a neural chip are main block of ANN. In a simple demonstration, we to tend to provide a sine wave to an exotic circuit that resulted in a distorted circular function wave shape. Forecast: Neural networks will evaluate future values from available and previous input signals. The target value is available input signals and delayed model of the input signals is given as input to the neural network. The neural network functions to predict the present input signal to operate the error toward zero. Fig.2. Depicts for design and validations of model using ANN chip, the sine wave is applied to find the unknown circuit and it is resulted in a erroneous sine wave. The output of the unknown system is the input to the target of the ANN chip to measure the correct the erroneous signals which is output of the processing unit in ANN chip

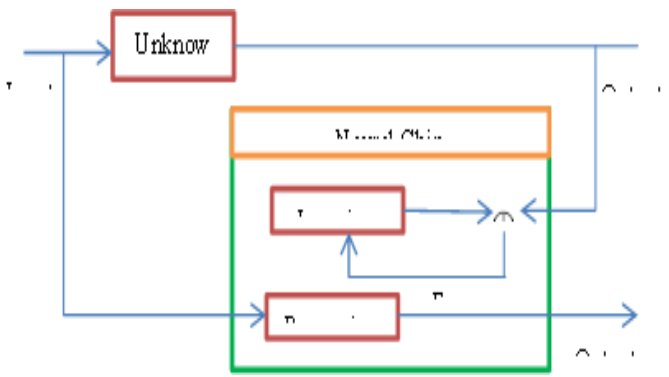

Fig.1. *Design of prediction for error while training the network*

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Prediction: ANN system can assess future qualities from present and past information signals. The objective worth is the present information signals and a postponed rendition of the information sign fills in as a contribution to the neural system. The neural system attempts to foresee the present info signal so as to drive the mistake toward zero. The prediction for error calculation is appeared in Fig.1 and the outcome is appeared in Fig.2. In this examination, the yield of the handling unit of the neural chip must be in front of the information signal. The test outcomes exhibit the fruitful expectation capacity of the neural chip.

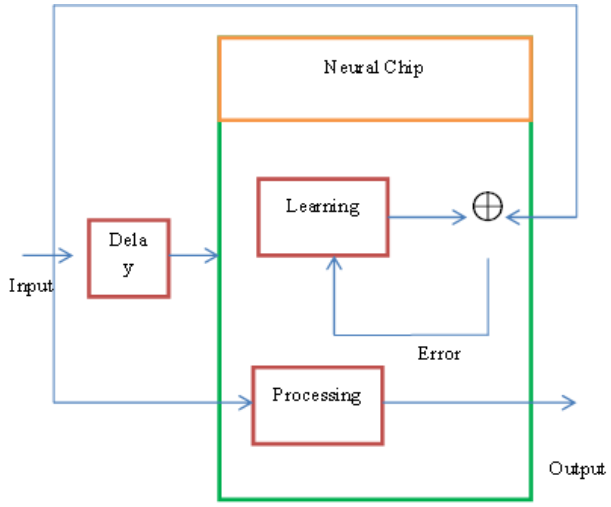

***Fig.2**. Design of modeling of the system for number of iterations*

Opposite demonstrating: In this application, the neural system endeavors to recoup a deferred adaptation of the sign, which is accepted to have been changed by an obscure Plant with added substance clamor. The yield of the obscure plant is the contribution to the neural system. The deferred obscure plant's info is the objective estimation of the neural system. The learning calculation renders the mistake little, and prompts the neural system to build up the converse model of the obscure plant. In Fig.2, the yield of the preparing unit of the neural chip must be a fittingly postponed duplicate of the information signal. In the sine wave explore, the yield of the neural chip turns into the info signal as shown the outcome is appeared in Fig.3.

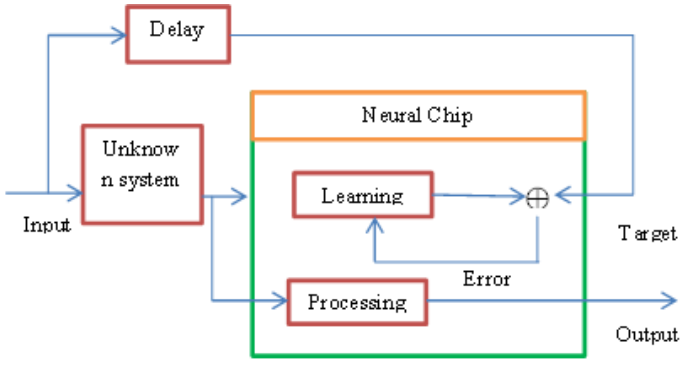

***Fig.3**. Design of Inverse Modeling to monitor the target output*

In this demonstration, the outcome of the process unit of the neural chip needs to be prior to the input. The experimental outputs signify the outstanding forecasts' ability CRF the neural chip. Counter modeling: during this application, the neural network strives to retrieve a delayed model of the signal that is assumed to possess altered unrecognized Plant with additive disturbance. The outcome of the unidentified plant is input to the neural network. The retarded unrecognized plant's input is the target value of the neural network. Therefore learning design statute contributes a small error, and cause the neural network to enlarge the counter model of the unknown plant. In Figure 6, the outcome of the process unit of the neural chip has got as roughly retarded version of the input. In the sine wave demonstration, the outcome of the neural chip becomes the input. A revised learning guild line is used to execute standard feed forward ANNs with learning to be used in accommodate signal process. The standard chip includes a feed forward network with learning circuits and a consistent. Network that uses a duplicate of the loads for process. The networks with learning circuits are perceived and checked output show that the learning circuits will simply learn the input-target temporal signals. This design is well scale3 to substantial networks and is feasible for large scale flexible signal process. The circuits are enforced on MOSIS little chips and therefore, the experimental results show their accomplished operations. Weight Update

- For every load conjunction it multiplies its output delta and input refreshing to induce the slope of the load.
- Bring the load in other way of the slope by removing a quantitative relation of it from the weight. This quantitative relation affects the speed and standard of learning, and it's referred to as learning to rate. The indication of the gradient of a load indicates wherever the error is increasing, that's why the load should be updated within the other way. These phases go on replicating till the execution of the network is acceptable.

Fig 1 depicts the neural network. During this network, inputs v_l, v_2 concerns with the load matrix, then this load inputs of the adder are added up. The outcome produced by adder blocks is given to the nerve cell Activation outcome. The outcome of activation task is increased by the average once more, and given to the input structure of output layer. This layered design of neural network is enforced in VLSI exploiting analog parts. Gilbert cell multiplier factor, summer and differential amplifier are used for various blocks. To scale back the ability demand we've got designed the neural network using improved technology. The human brain is composed of neurons that convey stimulating signals for every alternative thereby making intelligent thoughts. The recursive version of a neural network (called a man-made neural network) additionally consists of neurons that send stimulating signals to one another. Hence top result's that the factitious neural network will approximate a consequence of multiple inputs and outputs. As a result, neural networks are often used for a range of information mining tasks, among that are categorization, pictorial modeling, assembling, task approximation, and statistic prediction. Neural networks are ordinarily used for image process. The projected neural design are capable of acting operations like wave learning, amplification and frequency multiplication and might even be used for analog signal process activities. Nowadays, power has become one of the foremost necessary paradigms of style

convergence for multi-rate communication systems like optical information links, wireless merchandise, microchip & ASIC/SOC styles. With the arrival of the latest technologies and advancement in life science we to tend to try to operate the data by artificial means as our biological process perform within our body. Artificial intelligence along a biological word is perceived based on mathematical equations and artificial neurons. Our foremost aim is on the execution of neural specification (NNA) with on chip learning in analog VLSI for generic signal process applications. In this propounded paper analog parts like Gilbert Cell multiplier factor (GCM), nerve cell activation function (NAF) are used perform artificial NNA. The analog part used contains multipliers and summers beside the tan-sigmoid function circuit utilizing MOS semiconductor in sub threshold region. This neural design is trained utilizing Back propagation (BP) rule in analog domain with the latest approach of load storage. Layout sketch and authentication of the projected model is exploited using Cadence analog 1.6.4 tool. The technology utilized in planning the layouts is MOSIS/HP 0.5u SCN3M, Tight Metal. Due to the high-speed approach in integration technologies, wide-reaching systems models in brief due to the arrival of VLSI Technology the industry has attained an outstanding growth over the past 20 years. The quantity of applications of integrated circuits in superior evaluating, telecommunications, and client physical science has been rising quickly and systematically. Typically, the desired process power (or, in alternative words, the intelligence) of those applications is the propulsion for the quick development of this field. This stratified structure of neural network is enforced in VLSI utilizing analog elements. Gilbert cell multiplier factor, summer and differential electronic equipment is used for various blocks. To scale back the facility demand we've got designed the neural network utilizing advanced technology. The human brain is composed of neurons that send activation signals for every alternative thereby making intelligent thoughts. The recursive version of a neural network (called an artificial neural network) additionally consists of neurons that send activation signals to at least one another. Conclusion is the false (artificial) neural network can estimate the consequences of multiple inputs and outputs. As a result, neural networks are often used for different information mining tasks, among that are categorization, pictorial designing, assembling, task estimation, and statistic forecast. In image process neural networks are normally used. The projected neural design are capable of executing behavior like wave learning, amplification and frequency multiplication and might even be used for analog signal process tasks. Currently, power has become one in all the foremost vital prototype of model convergence for multi-GHz communication systems like optical information links, wireless merchandise, microchip & ASIC/SOC models. Since the Gilbert's Mixer helpful in frequency conversion in communication system, it's required to model MIXER for contemporary communication engineering applications with minimized power, high reliability and low interference. This paper presents model feature for layout model of Gilbert cell utilizes VLSI technology. The planning method, at numerous levels, is sometimes organic process in nature. It starts with a given set of demand. Once the necessities aren't met, the planning needs to be enhanced. Further, rationalized aspect of the VLSI technology is composed of assorted characterization, generalization of model, logic circuits, CMOS circuits and physical layout. The Gilbert Mixer (cell) is employed as number block. The major constituent of Gilbert cell is numerical couple transistors and current reflector circuit. In the propounded work Gilbert cell serves as multiplier and summer blocks of Neural Network. A mixer with a distinct RF signal is termed a single-balanced mixer. AN illustration is shown on figure 1. This design is often used because it is more prone to noise within the LO signal. Its major disadvantage is the LO-IF feed through. That is, the LO signal may discharge into the IF the IF isn't lower than the LO frequency. The low pass filter ensuing the mixer might not properly conceal the LO signal while not moving the IF signal. Double Balanced Mixers are used to stop LO product from reaching the output. It is necessarily 2 single-balanced circuits along with RF transistors connected in parallel and the switch pair is connected in anti-parallel. Therefore, the LO terms add to zero, and therefore, the RF signal doubled within the output. This arrangement provides a high level of LO-IF isolation mitigating filtering necessities at the output. Double balanced mixers are less prone to noise than the single-balanced mixers due to the differential RF signal. Figure 3 shows a double balanced mixer, it's additionally referred to as the Gilbert Cell Mixer. Mixers are used for frequency conversions, they transform the RF frequency to the IF frequency by multiplying it with the LO frequency.

3. RESULTS AND DISCUSSION

A multilayer perceptron is a feed-forward fake neural system design mapping sets of vitality esteems acquired from wavelet sub-band deteriorations. These vitality esteems are bolstered to the information layer and duplicated with introductory loads as given by Eq (4). The back-propagation is the all-inclusive rendition of straight perceptron considering its utilization of two concealed layers with nonlinear initiation work by the direct perceptron. The back-propagation in a neural system is the broadly connected learning calculation for multilayer perceptron. The back-propagation utilizes angle plunge for limiting the squared mistake between the system yield esteem and the ideal yield esteem. The got blunder sign are cast to compute the weight refreshes which speak to the intensity of information obtained on the system. Fig.4. portrays the engineering of MLP design. In back-propagation, the loads are refreshed after each example and by taking one example m at once as pursues:

3.1 Forward Phase

Apply the pattern $X_j^{(l)}$ to the input layer and propagate thec signal forward through the network until the final outputs X_j^L have been calculated for each i and L

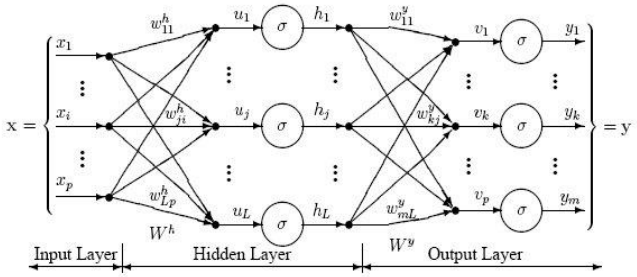

Fig.4*. Multilayer Perceptron architecture*

$$X_j^{(l)} = \theta\left(s_j^{(l)}\right) = \theta\left(\sum_{i=0}^{D(L-1)} x_j^{(l)} w_j^{(l)} + w_j^{(l)}\right) \quad (1)$$

Where D (L-1) is the number of neurons in layer (L-1), $X_i^{(l-1)}$ the output of the j[th] neuron in the (l-1)[th] layer, W_{ij} (i) synaptic weight contained in the current neuron, W_{ij} (i) current neuron's bias weight, $X_j^{(l)}$ output of the current neuron.

3.2 Back Propagation

In this, the loads and inclinations are refreshed based on the mistake slope drop vector. A system yield vector is acquired after the utilization of an info vector during the forward calculation stage. An objective vector is given to the system, to drive the yield of the system towards, the normal objective worth. Beginning with the yield layer and moving back towards the information layer, the blunder terms and inclination are determined as pursues:

$$e_j^{(l)} = \begin{cases} \left(u - x_j^{(l)}\right) & \text{for} \quad l = L \\ \sum w_{ij}^{(l+1)} s_j^{(l+1)} & \text{for} \quad l = 1,2,3, \ldots\ldots L-1 \end{cases} \quad (2)$$

where e_j^l is the error term for j[th] neuron in the l[th] layer

$$s_j^{(l=1)} = e_j^{(l+1)} \theta(s_j^{(l)}) \quad \text{for} \quad l = 1,2,\ldots, \quad (3)$$

where $\theta(s_j^{(l)})$ is the derivative if the activation function.

calculate the changes for all the weights are calculated as follows:

$$\Delta w_{ij}^{(l)} = \eta\, s_j^{(l)} x_j^{(l-1)} \ldots\ldots l.=1,2,\ldots\ldots L \quad (4)$$

where η is the learning rate. Update all the weights as follows:

$$w_{ij}^{(l)}(L+1) = w_{ij}^{(l)}(L) + \Delta w_{ij}^{(l)}(L)$$

where l=1, 2...L [(l)] and j=0, 1 ...L [(l-1)], W_{ij} [(l)] (L) is the current synaptic weight.

W_{ij} [(l)] (L+1) is the refreshed synaptic loads for use in the consequent feed-forward cycle. It is the full cycle of the period; the term time frame is utilized in neural systems preparing for portraying a total go through all the preparation designs. The weight in the neural net might be refreshed after each example is exhibited to the net, or only once toward the finish of the period. The total design is prepared every one of the qualities for arrangement of chose pictures from the database into typical or unusual. Multilayer perceptron design has been prepared in the system a forward way from the information layer to the yield layer. This yield is contrasted with objective reference esteems with discover any blunders utilizing the mean square mistake (MSE) and it is given by

$MSE = \sum_i error(d^i - y^i) = \sum_i ||\, d^i - y^i||^2$ The error can be reduced by passing the error from the output layer to hidden layer and then to input layer using back propagation ANN and at input layer the weights are updated. n = i1*w1+ i2*w2 (1). The Fig.4 shown the transistors level schematic diagram for single neuron and its layout design and its DRC results using Cadence Virtoso tool by using 32nm technology which is based on FinFET transistors.

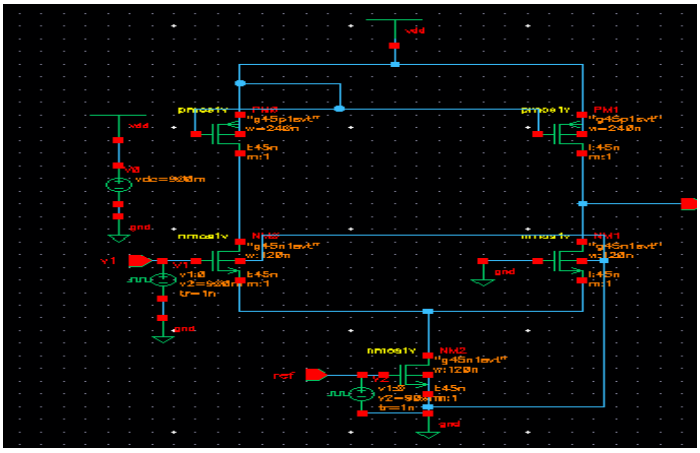

Fig.5(a). *Schematic circuit of single neuron and layout diagram and its DRC results*

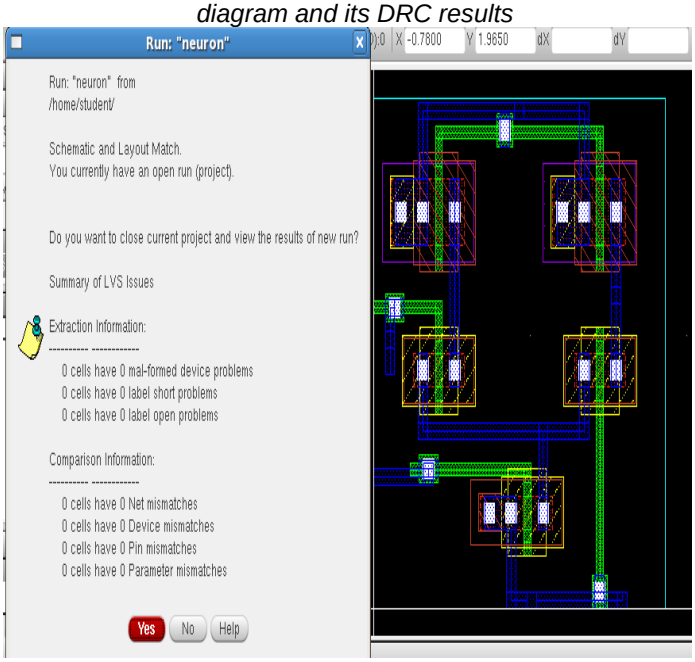

Fig.5(b). *Schematic circuit of single neuron and layout diagram and its DRC results*

Fig.5. shows the design for single neuron using FinFET technology contains five transistors of length L=45nm and width W=240nm. The designed circuit is simulated in FinFET package library to verify the compression of data; it is found that, almost 12% of data is compression. Single neuron schematic cell is converted into layouts and validated using DRC error is shown in Fig.5.

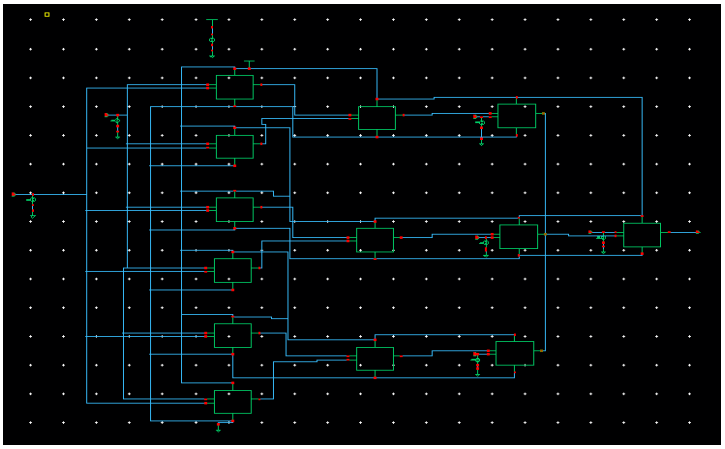

***Fig. 6**. Block level design of signal compression using ANN in Virtuoso tool*

The Fig.6 has shown the block level schematic diagram for compression using Cadence Virtoso tool by using 32nm technology which is based on FinFET transistors. This design is simulated and obtained results are shown Fig.7.

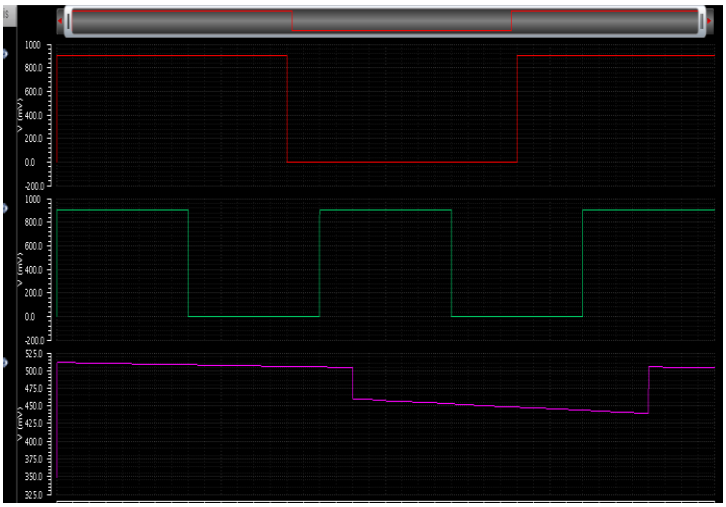

***Fig.7.** Simulated result of Signal compression using ANN*

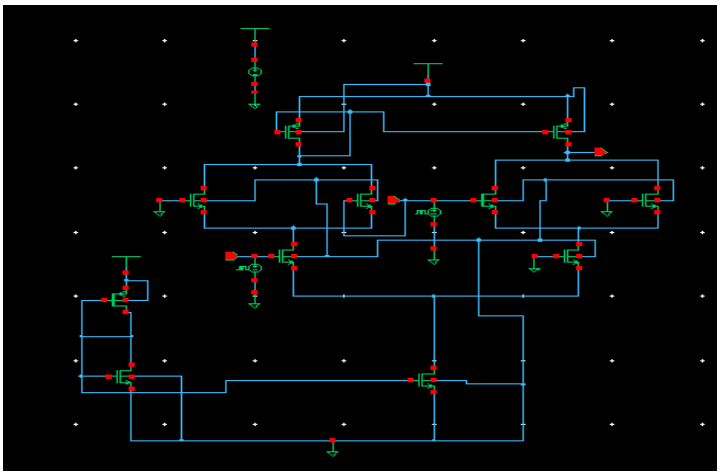

***Fig.8 (a).** Schematic circuit of Gilbert cell multiplier factor and its simulated results*

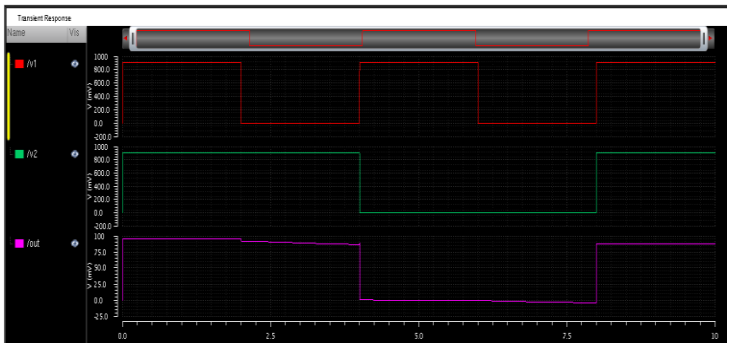

***Fig.8 (b).** Schematic circuit of Gilbert cell multiplier factor and its simulated results*

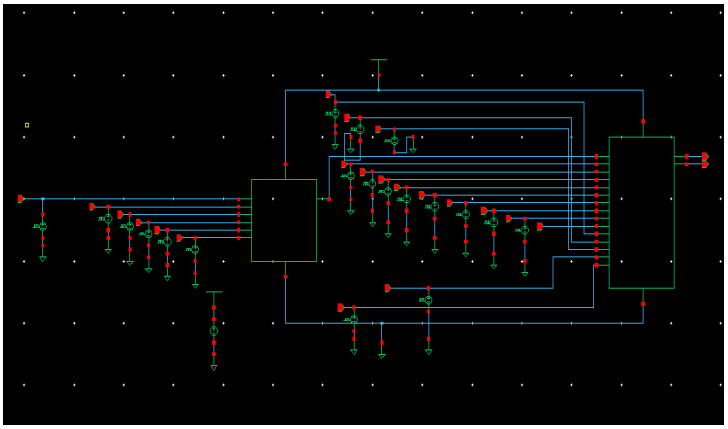

***Fig. 9**. Top module schematic design with test bench input signals*

*P=Proposed and **E=Existing

***Table.1**. Comparative table for the proposed work in terms of power, delay and area with existing work*

Design	Power		Delay (usec)		Area	
	*P	**E	*P	**E	*P	**E
Single Neuron	6.2mW	8.3mW 15]	3.9	5.19	20.35 sqm	31.2 sqm
Gilbert cell multiplier	9.4mW	12.1m W[14]	4.17	6.10	22.01 sqm	21.41sqm
Compression	17mW	15.2m W[10]	11.12	16.42	50.12 sqm	52.2 sqm
Decompression	12mW	9.3mW [12]	14.5	18.34	47.35 sqm	53.12sqm
Overall ANN	30mW	35mW [9]	130	180	95.45 sqm	230.23sqm

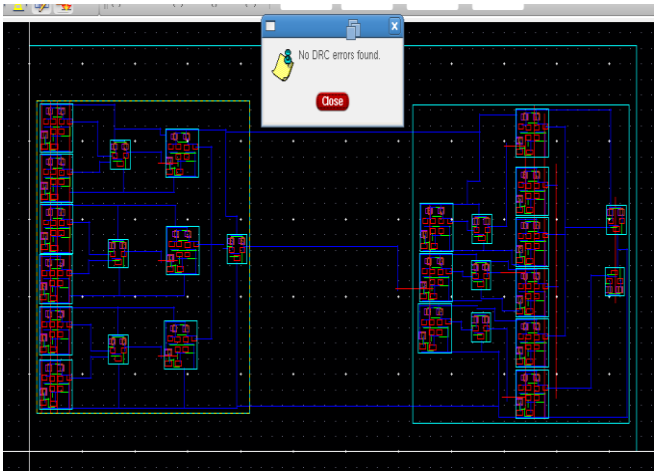

Fig. 10. *Compression top module layout design with DRC results*

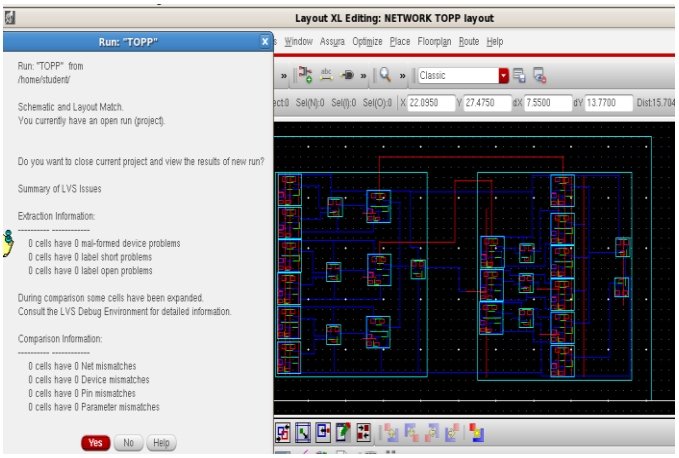

Fig. 11*. Top module layout design with LVS results*

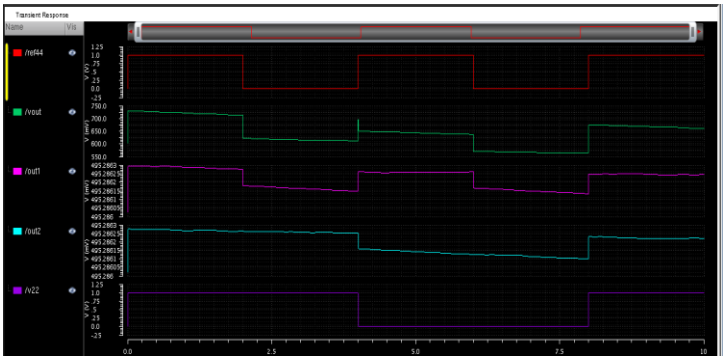

Fig. 12. *Simulated results of top module for signal compression*

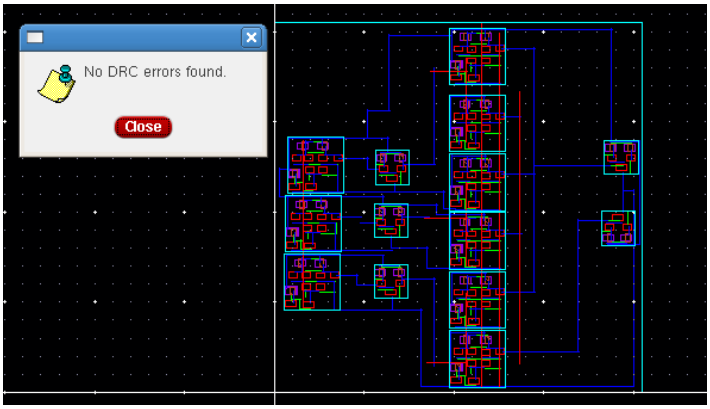

Fig. 13. *Decompression top module layout design with DRC results*

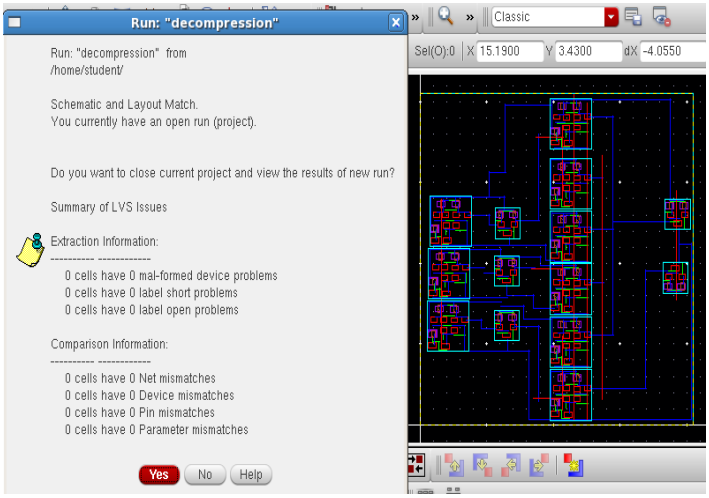

Fig. 14. *Decompression top module layout design with LVS results*

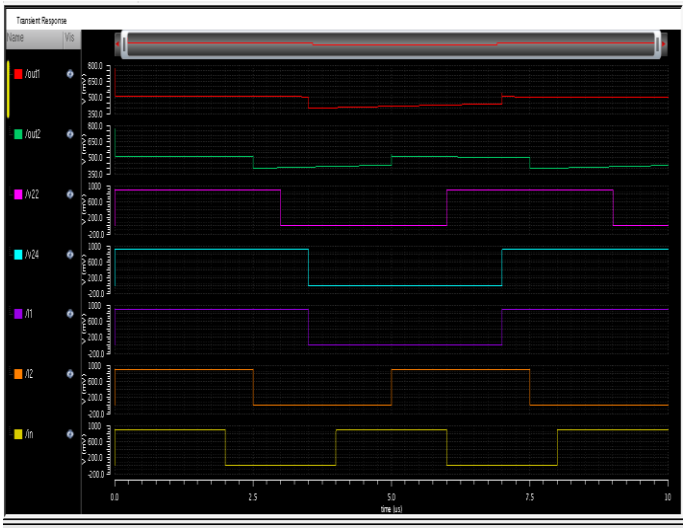

Fig. 15. *Simulated results of top module for signal decompression*

The proposed design for data compression decompression using ANN is successfully designed and simulated in Virtuoso Cadence tool, the obtained compressed and decompressed its DRC are shown in Fig.8 to Fig.15. The Pulse single

information given to the system was a heartbeat wave with v1 connected as .5 Vpp and recurrence 50KHz and v_2 was associated with ground. The system was prepared for the sine wave yield with same recurrence and sufficiency. As can be found in the Fig. 6 the yield unmistakably pursues the objective connected for the circuit for learning. In a manner the system figured out how to recreate the info sine wave as a yield. The system was made to learn 10 MHz recurrence sine wave with. 5 V pp amplitude appeared in Fig.7. The system steadfastly imitated the ideal objective of 10 MHz recurrence. The yield swing was from +.5 V and - .5 V. The union time for 10 MHz was determined as 200 ns with 1% blunder concerning sufficiency. The Neural system was tested for age of sine wave recurrence and sufficiency, more prominent than the info signal. Figure 24 demonstrates the outcome for the 100 KHz yield created from a 50 KHz information. The info v_1 was a sine wave with 50 KHz recurrence and .5 Vpp sufficiency. The Neural Architecture is reached out for the use of picture pressure and decompression. The recreation result for picture pressure and decompression are appeared in the Fig.14. The information v_1 was a sine wave with 1 Vpp voltage 5 MHz recurrence and v2 was a sine wave with .5 Vpp voltage and 10 MHz recurrence. The packed yield was a DC sign of 233.63 nV. The decompressed yield is appeared in a similar window figure 25. The decompressed yield for v_1 was a 1.2 Vpp sine wave with 5 MHz recurrence and v2 was a .51 Vpp sine wave with 10 MHz recurrence. As there is one yield for 2 contributions there is a half pressure.

5 Conclusion

Gilbert cell multiplier factor was laid out with info degree and farthest yield swing of 1.4V Neuron cell Activation result was intended for information shifts of ±3V and yield scope of 2.5 Uttermost separations current yields fluctuate 1 small scale amperes. A Neural structure was propounded using these parts. The Neural structure chips away at the accessibility voltage ±3 V with the yield swing of ±2.8V. Back Propagation algorithmic program was utilized for the training of the system. The sketched out neural plan had a union time of 200ns for simple contribution with 1% mistake. The Neural system was delineated as supportive for advanced and simple activities. The plan propounded will be utilized with option existing engineering for neural procedure. Half pressure was accomplished utilizing propounded neural structure. A changed learning guideline is utilized to execute particular feed forward ANNs with learning for use in versatile sign preparing. The measured chip incorporates a feed forward coordinate with learning circuits and an indistinguishable forward system which uses a duplicate of the loads for handling. The systems with learning circuits have been acknowledged and test outcomes demonstrate that the learning circuits can without much of a stretch become familiar with the info target fleeting sign. This design is effectively scale3 to huge systems and is feasible for huge scale versatile sign handling. The circuits have been actualized on MOSIS Tiny chips and the test outcomes demonstrate their effective tasks

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