

Design And Simulation Of Quantum Adder Using Ibm Quantum Experience

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Abstract: The use of unique quantum mechanical properties, such as superposition and entanglement, makes the quantum machines used to carry out operations with information. The fundamental theory of quantum computation is that the quantum belongings of particles can be used to symbolize and organize data. In conventional system, there are only two possible states either 1 or 0 that is stored in memory cells. But in the case of quantum system, the so called qubit, which holds 1 or 0 or a superposition of both. Moore who has predicted that quantity of transistors gets doubled for every 18 months in an IC. Now 5 nm node is the technology node followed by 7nm. Classical adder is made of CMOS transistor, further shrinking leads to quantum behavior as it is limited by the phenomena called quantum tunneling. Like classical gates such as OR, AND, NOT, NOR, NAND, EXOR, whereas in quantum, make use of X gate, Hadamard (H) gate, Z gate, S gate, T gate, Toffoli (CCNOT) gate. Operations like addition, subtraction, multiplication, etc can be done in quantum computing. The proposed quantum full adder is designed and simulated in IBM quantum experience.

Index Terms: Full Adder, Moore's Law, Qubit, Quantum computing, Quantum gates, Quantum mechanics.

1 INTRODUCTION

BACED on the prediction made by Gordon Moore, the complexity of the silicon chip doubles for every 18 months roughly [1]. The perception is named after Gordon Moore, the fellow benefactor of Fairchild Semiconductor and Intel, whose 1965 paper portrayed above observation, and anticipated this pace of development, would proceed for minimum one more decade. In 1975, anticipating the following decade, he reconsidered the conjecture to multiplying at regular intervals of every 24 months [2]. The period is frequently cited as a year and a half due to Intel official David House, who anticipated that chip execution would increase for 18 months (being a blend of the impact of more transistors and the transistors being quicker). Moore's law about the incredibly quick development of figuring power dependent on the quantity of transistors, and the breaking points of such extension, is more muddled than it might appear. Moore's perception formed our lives, contacting pretty much every part of it. What was similarly intriguing about Moore's Law is that it didn't pursue any logical standard. Moore's law isn't actually a law so much as a projection, but the things that make projection inaccurate remain a question. The IBM break through show for the first time the ability to detect and measure the two types of quantum errors (bit-flip and phase-flip) that will occur in any real quantum computer [3]. As of not long ago, it was just conceivable to address one sort of quantum error or the other, however never both simultaneously. This is a vital advance toward quantum error adjustment, which is a basic prerequisite for building a down to earth quantum system. It is as yet hard to state if quantum computing to turn into a reality, be that as it may, on the off chance that it does, Moore's law will probably vanish. In conventional system the information stored in a memory as a binary digits such as 1 or 0 whereas in a quantum system the information are represented as qubit, usually group of qubits [4].

The key point here it is, a solitary qubit can be expressed to a 1 or 0, or superposition of 1 or 0, the result obtained after measurement. So two qubits system has 4 different states simultaneously and three qubits has eight different states simultaneously, whereas conventional system has only one state among n possible states [5]. When all is said in done, a quantum system with n qubits can be in a self-assertive superposition of up to 2^n different states. A quantum system works on its qubits utilizing quantum logic gates and estimation, which likewise adjust the estimated state [6]. The computation is made out of a fixed succession of quantum rationale gates and an issue is encoded by setting the underlying estimations of the qubits [7], like how the conventional system functions. Quantum computations are frequently probabilistic, in that they furnish the right arrangement just with a specific known randomness. The point here to be noted down is non-deterministic and probabilistic computing is two different subjects, the term non-deterministic has an alternate meaning in software engineering.

2 EXISTING SYSTEM

2.1 Adder

To accomplish addition of numbers the digital hardware adder has been used. In numerous systems and different sorts of processors adders are utilized ALU. They are likewise used in different pieces of the processor, where they are utilized to ascertain addresses, table indexing, addition and decrement operations, and comparative activities [8].

2.2 Full Adder

A full adder, shown in Fig. 1, takes three inputs including carry-in from external circuits and produces sum bit with carry-out bit, the inputs are represented usually by A, B and C_{in} and outputs as S (Sum bit) and C_{out} , in decimal system the Sum is represented by $T_{FA} = 2 \times T_{XOR} = 2 D$. The importance of carry-in and carry-out in a full adder is used to connect cascaded full adder in the design process of n-bit adder [9].

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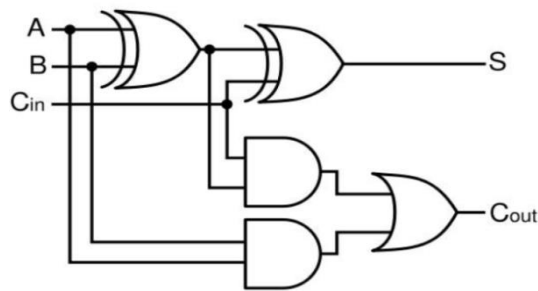


Fig. 1 Full Adder

The 1-bit FA (Full Adder) can be realized from numerous points of view, for example, with a custom transistor-level circuit or made out of different gate level implementation [10]. One such realization is using two half adders and one AND gate to implement FA, given by $S = (A \oplus B \oplus Cin)$ and $Cout = (A \cdot B) + (Cin \cdot (A \oplus B))$. In this realization, the last OR logic gate before the Cout might be supplanted by a XOR logic gate without changing the subsequent logic [11]. The critical path of a carry runs through 1 XOR-gate in adder and through 2 gates (AND and OR) in carry-block and therefore, if AND or OR gates takes 1 delay to complete, circuit has a delay of $T_C = T_{XOR} + T_{AND} + T_{OR} = D + D + D = 3D$.

2.3 Technologies

In semiconductor manufacture, the International Technology Roadmap for Semiconductors (ITRS) characterizes the 10 nanometer (10 nm) technology as the transistor size following the 14 nm technology. "10 nm class" means chips made utilizing process innovations somewhere in the range of 10 and 20 nm. While the guide has been founded on the proceeding with expansion of CMOS innovation, even this guide doesn't ensure that silicon-based CMOS will expand that far. This is not out of the ordinary, since the logic gate length for this node might be littler than 6 nm, and the comparing door dielectric thickness would downsize to a monolayer or even less. Researchers have evaluated that transistors at these measurements are altogether influenced by quantum tunneling. Subsequently, non-silicon augmentations of CMOS, utilizing III-V materials or carbon nanotube/nanowires, just as non-CMOS stages, including sub-atomic gadgets, turn based figuring, and single-electron devises, have been proposed. Henceforth, this technology denotes the down to earth start of nanoelectronics.

3 PROPOSED METHOD

Quantum computation framework outfitting the rule of quantum-mechanical marvels, for example, superposition and entanglement to perform tasks on information.

3.1 Quantum Superposition

Superposition is one of the key point in quantum mechanics which is like wave behavior in conventional science i.e., quantum bits existing in any of the two states or the combinational 2^n states simultaneously. Numerically, it alludes to a property of solutions for the Schrödinger condition; since the Schrödinger condition is straight, any direct blend of arrangements will likewise be a solution.

3.2 Quantum Entanglement

Quantum entanglement is a physical concept that happens when group of particles are produced or interrelated in manners with the end goal that the quantum condition of every particle can't be depicted autonomously of the others, in any event, when the particles are isolated by an enormous separation rather, a quantum state must be portrayed for the framework overall. It is entirely basic. The data for a qubit in some particle will be its spin state. In quantum mechanics, spin is the same than position, speed, vitality, and so on. That is, it can't be realized what state it is in precisely on the grounds that it's in a superposition of states. It's connected to some degree to Heisenberg's uncertainty guideline.

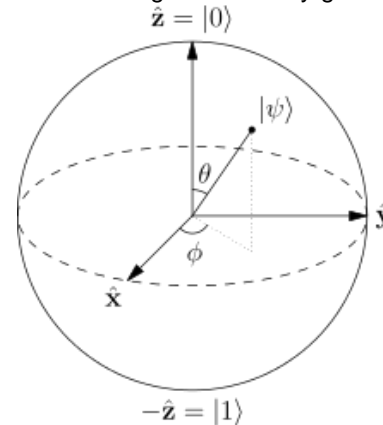


Fig. 2 Bloch Sphere

In Fig. 2, the z-axis uses for measurement basis. So the vector $|\psi\rangle$ has some polar angle θ , and its projection onto the z-axis (since measuring is done according to the z-basis). But of course, it's not fully in the zero or one state, it's partially in both.

3.3 Physical Realization

IBM recently managed to store a bit on a single atom of Holmium with the state defined by the magnetic pole orientation. The team used liquid helium to keep the atom's magnetic orientation stable long enough to read and write to it reliably with a nanoscope (scanning tunneling microscope). Reading data from an atom comes down to basic physics—all electrons have magnetic fields. If an electron is placed in another magnetic field, it'll align with that field based on their positive and negative "sides" of magnetism causing spin.

4 SIMULATION AND RESULT

Here the simulation of basic quantum gates and their corresponding output state and bloch sphere are illustrated. Basic Quantum gates are X, Hadamand, Z, Y, T, S.

4.1 X Gate

It is also known as an X-rotation, since it rotates the state by π radians around the X-axis. If the X gate is started with $|0\rangle$ state at the top of the Bloch sphere, the X gate rotates the bit to the bottom of the Bloch sphere ($|1\rangle$). See the below schematic and also try the X gate in the Composer, using the score below. The X gate design model in the quantum composer is shown is the Fig. 3.

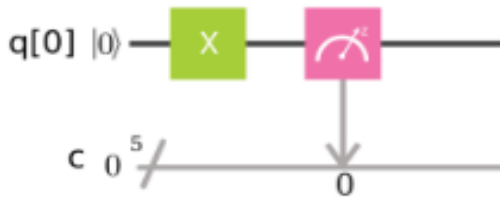


Fig. 3 Design for X Gate

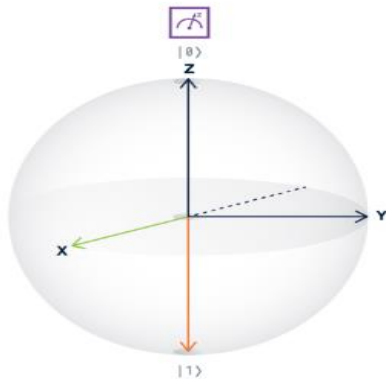


Fig. 4 Bloch Sphere for X Gate



Fig. 5 Output for X Gate

The Design for X gate with its corresponding Bloch Sphere and the output states of the bit are shown in the Fig. 4 and Fig. 5. Here the X gate is forced with bit 0 and the bit is flipped from positive Z axis to negative Z axis.

4.2 CNOT Gate

The notation for the state of a machine with multiple qubits is similar as before, but now there are multiple numbers inside the |> 'ket'. For a two-qubit processor, the qubits can be in four possible states: |00>, |01>, |10>, and |11>. Reading from left to right, the first number represents the state of the second qubit and the second number represents the state of the first qubit. That is to say: the first qubit (q[0]) is always listed at the far right. This notation is chosen to be consistent with the classical binary representation of numbers. Just like the single qubit, there can also be superpositions of these states like: $12\sqrt{(|00\rangle - |11\rangle)}$. When this state is measured, both qubits will have the same value, but 50% of the time both will be 0 and 50% of the time both will be 1.

Table 1 Truth Table for Cnot Gate

Starting state	Ending State
00>	→ 00>
10>	→ 10>
01>	→ 11>
11>	→ 01>

The Controlled-NOT or CNOT is used for conditional gate. The truth table for the CNOT gate is given in Table 1.

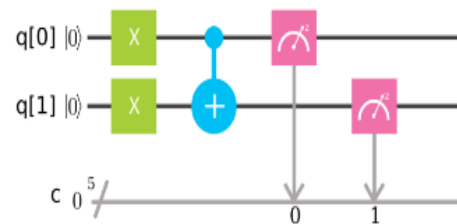


Fig. 6 Design for CNOT Gate

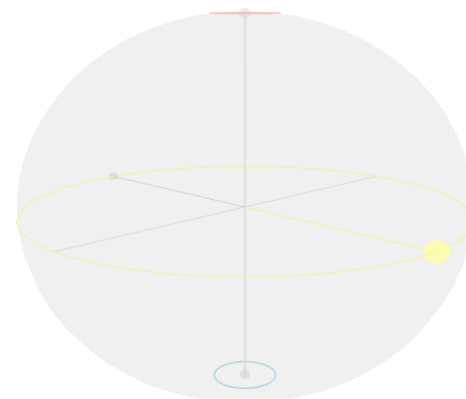


Fig. 7 Bloch Sphere for CNOT GATE

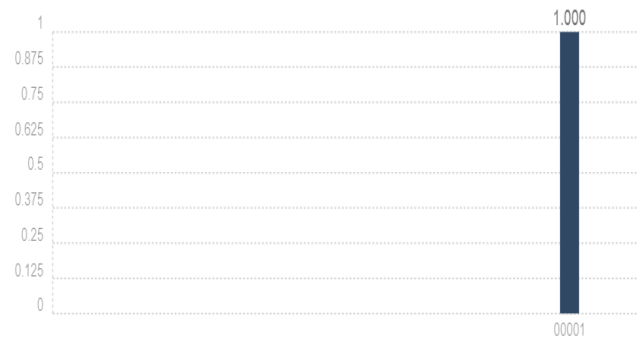


Fig. 8 Output for CNOT Gate

The Circuit for CNOT gate it's the corresponding Bloch Sphere and the output states of the bit is shown in the Fig. 6, Fig. 7 and Fig. 8. In the CNOT gate if the control bit is set then the CNOT gate flips the target bit and is appeared at the output.

Otherwise the target bit remains the same state.

4.3 Quantum Full Adder

In this proposed method, the full adder is designed by using two half adders. The half adder consists of Toffoli gate and CNOT gate. The Design for the full adder using a quantum gates is shown in the Fig. 9.

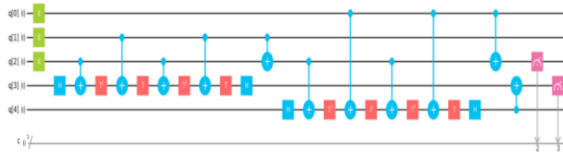


Fig. 9 Circuit for Full Adder



Fig. 10 Output for Full Adder

The output for the full adder using a quantum gates is shown in the Fig. 10. Here the carry and sum state appeared as 1 since the three inputs for the adder is 1.

5 CONCLUSION

Thus the design and simulation of quantum adder has been done successfully. The basic gates of the quantum computing are simulated and verified by their own logics individually. Quantum full adder is designed by using the basic quantum gates. And the simulation result of each gate has been noted clearly in Bloch sphere and corresponding output provided in bar-chart.

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