Analysis Of Scheduled Routing Algorithms On 5-Port Router For Network On Chip Application

Dharmavaram Asha Devi, Satyavati Jaga

Abstract— Network on Chip (NoC) is a trending technology with many advantages of reducing the latency and area. The proposed paper is analyzed the two popular scheduling algorithms, First In First Out (FIFO) and Round Robin for transmission of data packets within the network on chip. The proposed algorithms are developed in Verilog Hardware Description Language and analyzed in 28nm Technology. These scheduling algorithms are verified with NoC parameters: Latency, Throughput, Bandwidth, Bit rate and Baud rate. Here, five port routers have been considered for testing and verification of data packets. After the analysis of these two algorithms, round robin algorithm has given better results with less latency and high throughput. The proposed analysis is used in networking and on chip communication applications.

Index Terms— Baud rate, Bit rate, First In First Out, Hardware Description Language, Latency, Network on Chip, Round Robin.

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1 INTRODUCTION

NETWORK on Chip helps in organizing the communication between source and destination modules. The communication between modules will be through various routing paths and switches. It has number of point-to-point connections of data links through switches. In order to improve the efficiency of power, complex SoCs are replaced with NoCs. Therefore, operating frequencies can be improved. Then, it is easy to implement the network communication with lesser delays. Within the NoCs, routing concept is a key to improve the latency, area and throughput. The NoC can tested with many algorithms to know which algorithm suits the best. The parameters of NoC: Latency, Throughput, Bandwidth, Bitrate and Baudrate are analyzed with different algorithms. The parameter values are to be calculated to get the performance of the NoC.

i. Latency

The time taken by the task from source to destination is called as latency. It is a delay time to network. It is also an important parameter of NoC. It is to be reduced to get the best performance.

ii. Throughput

The number of data bits transmitted successfully in a given amount of time between source point to destination point is called throughput. It is an important parameter of NoC. It is calculated by number of tasks completed in unit time. Its formula is (information or data bits transmitted) / (time). Its units are bits per second.

iii. Bandwidth

The amount of data transmitted in fixed amount of time is called a bandwidth. It is bits per second or bytes per second. It gives the speed of a network. It gives the performance of NoC router.

iv. Bit rate

The rate at which amount of data bits transmitted is called a bit rate. It is a parameter of NoC to determine the performance of a system. It is always greater than or equal to baud rate. The calculation is also simple and can be calculated by using the formula:

Bitrate = total number of bits transmitted /second.

The relation between bit rate and baud rate is:

$$b = n*B.$$

Where, b = bit rate; n = total number of bits including redundant bits (start bit, stop bit and parity bit); B = baud rate;

v. Baud rate

The number of symbols transmitted per second is called as baud rate. It gives the signaling speed. It is always less than or equal to bit rate. It sends symbols which are group of bits made up of 0's or 1's. It also be calculated by using a formula:

Baudrate = total number of information bits transmitted/second.

The relation between baud rate and bit rate is:

$$B=b/n.$$

Where, B = baud rate; b = bit rate; n = number of bits.

In the proposed research work, we have analyzed the NoC parameters with respect to First In First Out and Round Robin algorithms. The organization of the paper is represented with seven sections including 1. introduction followed by 2. History of investigations, 3. Scheduling Algorithms for NoC, 4. First In First Out algorithm, 5. Round Robin algorithm, 6. Result analysis and 7. Conclusion.

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2 HISTORY OF INVESTIGATIONS

The SoC technology has issues like more physical connection, power consumption and delays. The parameters for On-Chip are not that great. The network on chip reduces the drawbacks of SoC by reducing delay, power consumption and physical connections.[2], this book gave the different routing algorithms for NoC that can be implemented to get better results. In [3], it is mentioned that the NoC has to be used for specific application. Therefore, it is to be made according to desired specifications. In [5], it is given that the implementation of scheduling algorithms is needed to achieve the desired results. The performance of NoC router is to be verified. Different architectures are mentioned. In [6], discussion about the area occupation and power consumption details of NoC. [7] gives the details how the Round robin is implemented with priority. [8], proposes about the area and power consumption for Round robin algorithm. This paper compares the parameters of NoC router for two algorithms FIFO and Round Robin algorithm.

3 SCHEDULING ALGORITHMS FOR NOC

The NoC router is implemented with various algorithms and they are First In First Out, Last In First Out, Priority algorithm and Round Robin. In the proposed paper, we have analyzed NoC parameters using to popular algorithms FIFO and Round Robin. These algorithms are discussed in following IV and V sections.

The First In First Out is like a queue. The task which comes first is completed first and is easy to implement. It does not include preemption. The FIFO is best implemented for small systems. The speed is also good for FIFO algorithm. The round robin is easy to implement and analyze. The preemption of task and priority for task are included in this algorithm. The time slot is shifted periodically with respect to priority.

4 FIRST IN FIRST OUT ALGORITHM

FIFO (First In First Out) is a basic, oldest and best algorithm. Its operation is like a queue. This is more suitable for small networks. It is easy and simpler way to implement and operate. Analyzation is also favorably good. But it has got its own demerits like, it does not allow preemption technique, waiting time is higher, there will be a load on the processor for maximum time. Therefore, speed cannot be improved if the network data is large and cannot get good throughput.

In the proposed system, five port routers are considered. Each data port can input 8 bits, out of which upper 3-bits indicates header bits and rest 5-bits are information bits. The header bits are used to identify the address of destination port. The data select input is used to select one of the ports from five input ports. The clock signal is used to run the blocks to maintain synchronism.

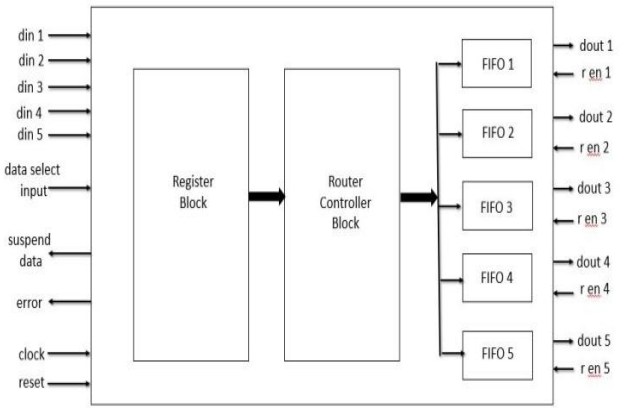

Fig 1. Block diagram of FIFO algorithm

The reset signal is used to restart the scheduling. The suspended data is high when there is any loss of data. The error signal is high when there is any error detection in transmitted data packet. This parity is checked and verified in the router controller block. The functional block diagram of FIFO algorithm is shown in Fig 1.

Register block

The register block consists of five registers, each with 8-bit size. This block is used for store and forward mechanism. The data packets are stored concurrently in the five stacked registers in the register block. The data packets are stored in order to verify whether there is any errors or data loss in transmitted packets.

Router controller block

This block is used to route the data packets according to the destination address in data packets. It checks whether the destination port is empty or not. If empty the data packet is sent to destination else the data packet is sent after the destination port is empty. The parity is internally verified within this block by using the Linear Feedback Shift Register (LFSR). If there is any error in the transmitted data packet then the error signal is made high otherwise it will be low. It also checks whether the data is lost or not. If data is lost then suspend data signal is made high otherwise it will be low.

There are five output ports, FIFO 1 to FIFO 5 to store the transmitted data bytes that are decided by the router controller block. The router controller fills the output FIFO registers according to priority indicated by 3 header bits. The read enable is made high when the data packet is transmitted to the output port.

The FIFO operation starts with clock and reset as shown in Fig 2. They help to restart and run the process accordingly. The data packets have header bits and transmitted to desired destination port. The router controller block checks whether the desired destination port is empty or not. If empty the data packet is sent and the data is read. Else data packet is sent when the destination port is made empty. The process is repeated for five ports in first cum first serve basis.

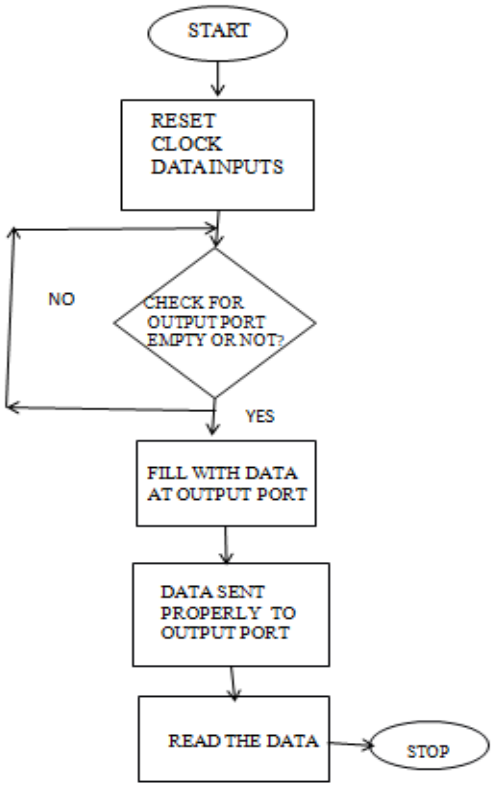

Fig 2. Flow chart of FIFO algorithm for NoC router

5 ROUND ROBIN ALGORITHM

It is also a good algorithm and simple to analyze. The processor utilization is very less. And it provides the preemption technique. In this algorithm priority of a task can be set. It improves speed and efficiency of system. It provides task with time slot duration. But the low priority task needs more time to perform.

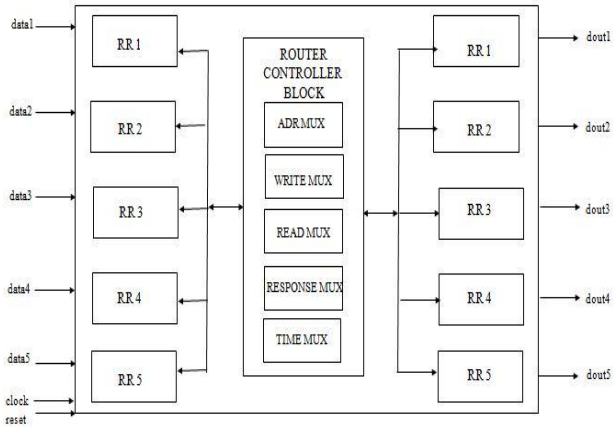

Fig 3. Block diagram of round robin algorithm

In this proposed paper, we have considered five port routers. There are five data an input with each data packet comprises of 8-bit information bits. It doesn't have any header bits. The reset signal is used to restart the block. The clock signal is supplied to other blocks to work synchronously. All the input ports can be loaded with data packets at same time. The priority is set to ports by using LSB priority technique or we can use MSB priority technique. In this algorithm we implemented priority with LSB. The data transmission is one to one transmission i.e. if input port-1 gets the data it has to send to output port-1.

5.1. Router controller block

a) ADR MUX

The address multiplexer is used to connect ports with their respective output ports. It maps the input port-1 with output port-1, input port-2 with output port-2, input port-3 with output port-3 and follows. It generates the selections lines from the arbiter which is within the router controller block.

b) TIME MUX

The Time multiplexer used to make a comparison between the burst times and time quant. If the time quant is greater than burst time then the process executes for time quant time, else the process executes for series of time quant. It processes the data by comparison of time.

c) WRITE MUX

The write multiplexer enables to write the data on output port according to the selection lines obtained. When the corresponding output port is obtained, the data is written according to the time multiplexer.

d) READ MUX

The read multiplexer reads the data in the output port. The selection lines are obtained from arbiter within the router controller block.

e) RESPONSE MUX

It transmits the signal from output port to input port. When the complete data is transmitted, the response multiplexer sends the response signal to corresponding input port.

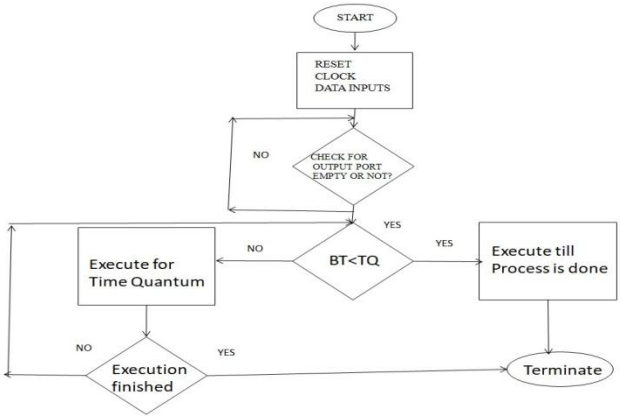

Fig 4. Flow chart of round robin algorithm for Round Robin algorithm

The output ports are register blocks which takes the data from the input port. When complete data is received, the response signal is sent to corresponding input signal.

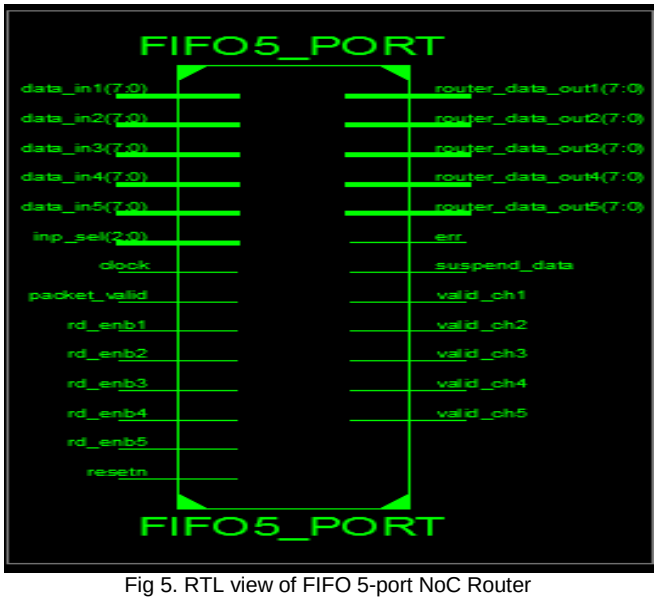

Fig 5. RTL view of FIFO 5-port NoC Router

The Round Robin algorithm starts with the reset and clock signals. The data packets are sent to output ports according to address multiplexer. The burst time and time quant are taken and decision is made between the burst time and time quant. If the time quant is less than burst time the process executes for series of time quant, else the process executes for remaining burst time and completes the process. After the data written, output ports are read. Accordingly, the response signal is sent to the input ports.

The RTL (Register Transfer Level) diagram of FIFO 5-port NoC Router is shown below in Fig 5. It is used in the Logical design of Integrated Circuit. It just gives the link flow between the NoC router hardware and the logic of the design. It is a graphical representation of FIFO scheduling algorithm.

6 Results and Discussion

The verification of FIFO is illustrated in Fig.6. From the Fig.6, it is clearly indicated as when inp-sel value is equal to zero, then the data_in1 value will be transferred to the output of the corresponding router. When the data packet is 001XXXXX, it goes to output port 2, packet valid is high, empty signal is high then data moved to corresponding output port, write signal is high, error signal is low, suspend data signal to low.

When the data packet is 010XXXXX, it goes to output port 3, packet valid is high, empty signal is high then data moved to corresponding output port, write signal is high, error signal is low, suspend data signal to low.

When the data packet is 011XXXXX, it goes to output port 4, packet valid is high, empty signal is high then data moved to corresponding output port, write signal is high, error signal is low, suspend data signal to low as shown in Fig.6.

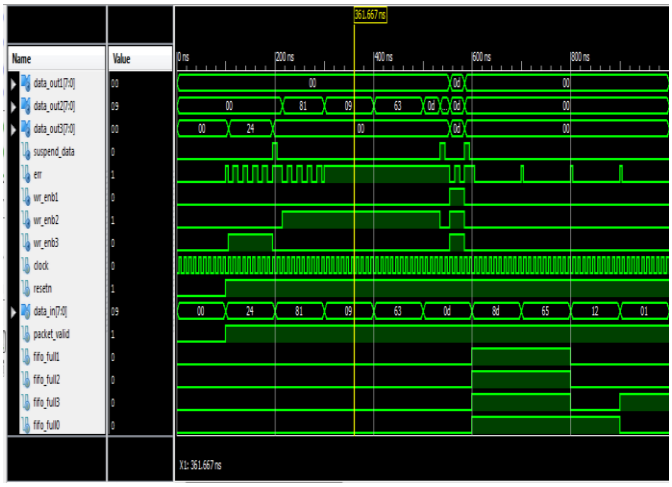

Fig 6. simulated waveforms of FIFO

Similarly, the round robin algorithm simulated result is shown in Fig.7. When the data packet is given to port 1 with some burst time to it. The selection lines are generated as 000. The time multiplexer, read multiplexer, write multiplexer, response multiplexer and address multiplexer will get the selection line is same as generated. The most priority port is first port. So according to burst and time slot, the data is transmitted among all other ports. After transmission of data, the response signal sent to port-1 as high.

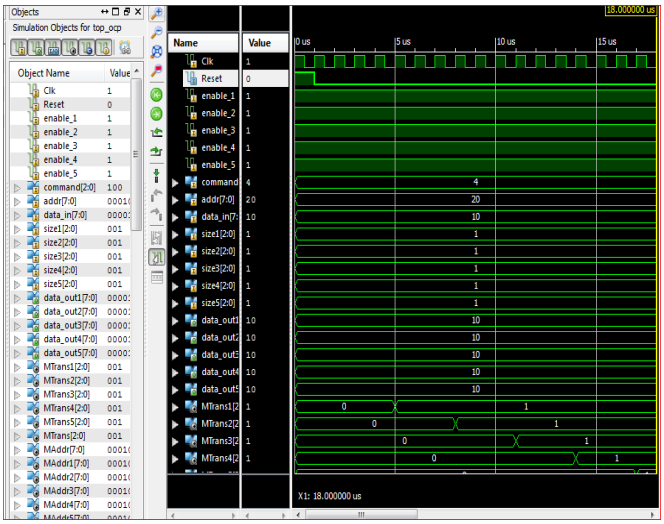

Fig 7. simulated waveforms of Round robin (time slot=1ns)

When the data packet is given to port 2 with burst time, then the selection lines are generated as 001. The time multiplexer, read multiplexer, write multiplexer, response multiplexer and address multiplexer will get the selection line, same as generated. The most priority port after first port is second port. Because, according to burst and time slot, the data is transmitted among all other ports. After transmission of data, the response signal is sent to port-2 as high.

When the data packet is given to port 3, with burst time, then the selection lines are generated as 010. The time multiplexer, read multiplexer, write multiplexer, response multiplexer and address

multiplexer will get the selection line is same as generated. The next priority after second port is third port. So, according to burst and time slot, the data is transmitted among all other ports. After transmission of data, the response signal will be sent to port-3 as high.

Similarly, when the data packet is given to port 4 with burst time, then selection lines generated as 011. All the multiplexers will get the selection line same as generated. And the next priority after third port is fourth port. Therefore, according to burst time slot, the data is transmitted among all other ports. After transmission of data, the response signal sent to port-4 as high.
When the data packet is given to port 5 with some burst time to it. The selection lines are generated as 100. The time multiplexer, read multiplexer, write multiplexer, response multiplexer and address multiplexer will get the selection line is same as generated. The least priority port is fifth port. So according to burst and time slot, the data is transmitted among all other ports. After transmission of data the response signal sent to port-5 as high.

From testing the NoC five port router with different algorithms, different results are obtained. The latency value for FIFO algorithm is good (9.126ns). The latency value for Round robin for the same time slot, is 8.667ns. The throughput is also good for the FIFO algorithms. The throughput value increased for the round robin as the delay is reduced. The area occupancy on a chip for FIFO algorithm is good as it occupies the 304 LUTs in total. The area occupancy on chip for round robin algorithm is decreased as the LUTs occupied are 45 in total. The maximum frequency for FIFO algorithm is up to 254.672MHz and for the round robin algorithm is up to 96.728MHz. Therefore, we can say that the round robin gave the good results compared with FIFO.

Table 1. Comparison analysis of FIFO and Round Robin

NoC Parameters	FIFO algorithm	Round Robin algorithm
Latency	9.126 ns	8.667 ns
Maximum frequency (fm)	127.336 MHz	48.364 MHz
Bandwidth (2*fm)	254.672 MHz	96.728 MHz
Throughput	800Mbps	800Mbps
LUTs	304	45
Bitrate	800Mbps (Tp=10ns)	800 Mbps(Tp=40ns)
Baudrate	500Mbps (Tp=10ns)	800Mbps (Tp=40ns)

7 Conclusion

A five-output port network router for network on chip with FIFO and Round Robin algorithms are successfully designed and its functional verification is done with codes written in Verilog HDL. Congestion is avoided by using store and forward type of packet-based protocol in FIFO algorithm. The latency values are good for both algorithms, but the Round Robin value is most choosy. The speed and efficiency parameters are good for the Round Robin algorithm. The desired results are obtained by testing the algorithms using Xilinx software tool.
The proposed work is designed with five ports. However, the number of ports can be enhanced by increasing the header bits and selection line bits to improve the router capacity. Throughput and latency values cab improved further by implementing combined scheduling algorithms.

Acknowledgment

The authors wish to thank SNIST and CBIT college managements, for the support and encouragement given for R&D activities.

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