Comparative Analysis Of Cmos Inverter For Low Leakage Power

Laxmi Kumre, Bhavana P Shrivastava, Neeraj Rai

Abstract: In CMOS circuits, the reduction of the threshold voltage due to voltage scaling leads to increase in sub threshold leakage current and hence, static power dissipates. In the nanometer technology regime, power dissipation and process parameter variations have emerged as major design considerations. These problems continue to grow with leakage power and become a dominant form of power consumption. On the other hand, variations in the device parameters both systematic and random, translate variations in circuit parameters like delay and leakage. Leakage power dissipation is projected to grow exponentially in the next decade according to the International Technology Roadmap for Semiconductors (ITRS). This directly affects portable battery operated devices such as cellular phones and PDA's since they have long idle times. In this paper several techniques have been analyzed for efficiently minimize the leakage power loss. Comparative analysis of CMOS inverter for low leakage power have been presented here and result shows that sleepy stack technique consumes 52% less power as compared to standard CMOS technique in 45nm technology.

Index Terms: CMOS inverter, Leakage power, static power dissipation, sleepy stack, forced NMOS transistor, technology scaling.

1. INTRODUCTION

AS technology scales down, the size of transistors has been shrinking. The number of transistors on chip has thus increased to improve the performance of circuits. The supply voltage, being one of the critical parameters, has also been reduced accordingly in order to maintain the characteristics of an MOS device. Therefore, in order to maintain the transistor switching speed, the threshold voltage is also scaled down at the same rate as the supply voltage. As a result, leakage currents increase dramatically with each technology generation [1]. For the high performance, high packing density and low power consumption results the deduction in transistor size and the scaling is required [2]. Using such type of technology, the leakage power of transistor increases exponentially when the technology is scaled, supply and threshold voltage also scaled. Due to reducing transistor size, the channel length also become short which increases the leakage current through a transistor in off condition. CMOS technology has been scaled down from 1µm to 45nm over the last decade. Technology scaling reduces the gate oxide thickness and the gate length thereby increasing the transistor density and also reduces the delay. Reduced gate lengths result in an increase in the leakage power dissipation. Increased transistor densities result in an increase in the power dissipation per unit area thereby creating hotspots. Scaling down the supply voltage reduces the switching power dissipation. Threshold voltage is simultaneously scaled down along with the supply voltage [3]. Scaling down the threshold voltage significantly increases the leakage power dissipation. Leakage power is a very serious problem in mobile application. So resolving this, different types of techniques are used at circuit level and process level. Low threshold voltage also results in increased sub threshold leakage current because transistors cannot be turned off completely [1],[2]. For this reason, static power consumption i.e., leakage power dissipation has become a significant portion of total power consumption for current future silicon technologies [4].

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2 PREVIOUS WORK

2.1 Conventional CMOS inverter approach

In the conventional CMOS inverter approach, pull-up network and pull-down network are used with two transistors. The pull-up network is called a PMOS transistor and pull-down network is called a NMOS transistor. Its operation can be understood with a simple switch model. The CMOS inverter transistor is nothing more than a switch with an infinite off resistance and a finite on-resistance. When input is logic 0, logic 1 is obtained at the output and when input is logic 1, logic 0 is observed at the output. CMOS inverter has three components of power – static power, dynamic capacitive power and dynamic short circuit power [5].

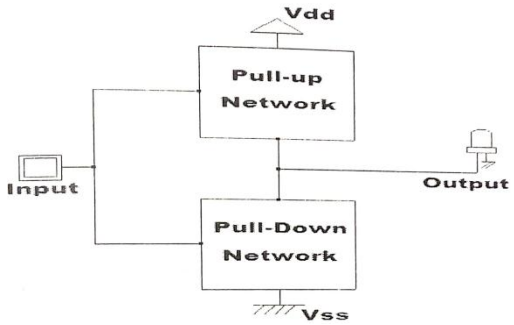

Figure 1 - Conventional CMOS inverter

Static power is due to leakage current and this current is determined by "off" transistor. It is given as,

$$P_{static} = V_{dd} \times I_{leakage}$$

where V_{dd} is a supply voltage and $I_{leakage}$ is a leakage current during the off transistor. Dynamic power is due to charging and discharging of load capacitance. It is given as,

$$P_{dynamic} = C_L \times V^2_{dd} \times f$$

where C_L is a load capacitance, V_{dd} is a supply voltage and f is a clock frequency.

2.2 Forced NMOS transistor inverter

This approach is same as conventional CMOS but with an added NMOS at the bottom. The two NMOS devices increase the delay which results in reduction in leakage power in the circuit. An extra NMOS decreases the $I_{leakage}$ through MOS device hence decreasing power consumption as compared to

the conventional CMOS [6] [9]. Fig.2 shows forced NMOS transistor inverter.

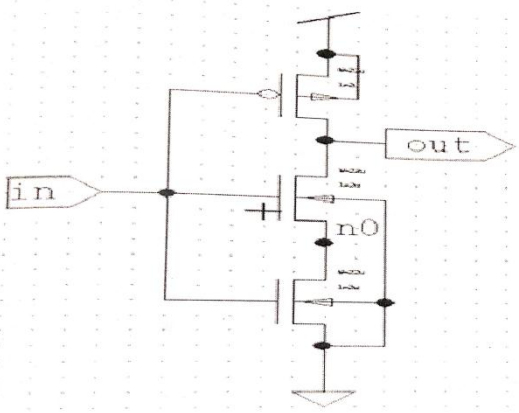

Figure 2 – Forced NMOS transistor

2.3 Forced PMOS transistor inverter

In this approach, the circuit consists of two PMOS and one NMOS. In other way, it can consider same as conventional CMOS but with an added PMOS at the top. Here the addition of two PMOS devices increases the delay which results in reduction in leakage power in the circuit [8]. Fig.3 shows forced NMOS technique.

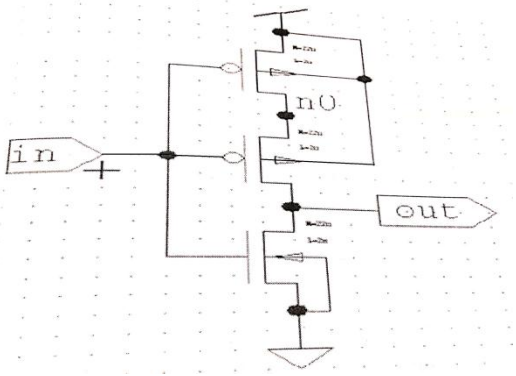

Figure 3 : Forced PMOS transistor

2.4 Forced 2-NMOS transistor inverter

This approach combine's property of both reduce swing as well forced NMOS inverters. The load PMOS transistor in the reduced swing inverter is always in saturation since $V_{gs} = V_{ds}$. It reduces the voltage at the source of the second PMOS in each inverter to approximately $V_{dd} - V_{tp}$ thus switching it off when the low - swing clock signal reaches its peak voltage [8]. This approach has low power consumption but with increased delay and layout area. The output voltage swings from 0 to $V_{dd} - V_{tp}$. PMOS acts as a load hence reduces voltage swing to $V_{dd} - V_{tp}$. This reduction in swing results in a reduced power consumption [7] [8]. Fig. 4 shows forced 2NMOS transistor inverter.

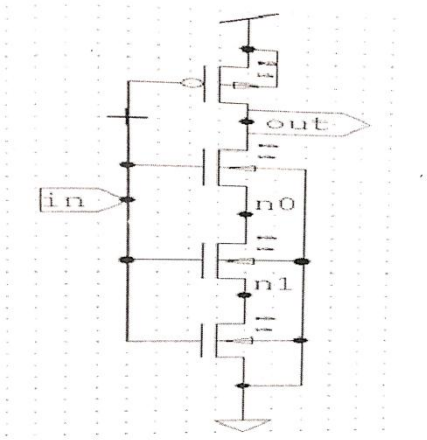

***Figure 4:** Forced 2 NMOS transistor*

2.5 Stack Approach

Another scheme for reducing leakage power is the stack approach, which uses a stack effect by breaking an existing transistor into two half size transistors to take advantage of the stack effect [4]. It is based on the principle that a PMOS and NMOS device can be replaced by two equal NMOS and PMOS devices of half W/L. Gate terminals of both NMOS as well as PMOS transistors are tied together and connected to a single source which serves as input for the inverter. Output is taken across a capacitor which serves as a load for the inverter circuit. However, divided transistors increase delay and could limit the usefulness of this approach [10]. Fig.5 shows the stack technique.

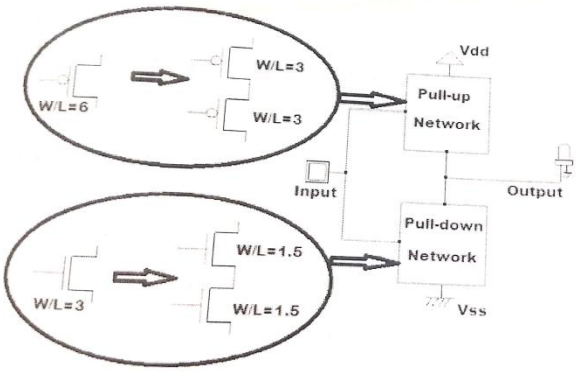

***Figure 5** : Stack transistor*

3 PROPOSED SLEEPY STACK APPROACH

The sleepy stack approach combines the sleep and stack approaches. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. Figure 6 shows its structure. It having the benefits of both stack and sleep techniques are used simultaneously in the sleepy stack approach. During the sleep mode, sleep transistor are turned ON and stacked transistor suppress the leakage current while saving the state. Each sleep transistors are placed parallel to one stack transistor which reduces the resistance of both transistor and thus delay is decreased during active mode. When sleep transistors are turned OFF, the existence path from V_{dd} or ground prevent the float in output and also in this case, leakage current further can be reduced by applying high threshold voltage on the sleep transistor and the transistor in

the parallel to the sleep transistor. In this approach, pull-up network is replaced by three transistor and similarly pull-down network is also replaced by three transistors and also additional wire is connected for S and S' which are sleep signal.During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a significant matter for this approach since every transistor is replaced by three transistors and since additional wires are added for S and S', which are sleep signals.

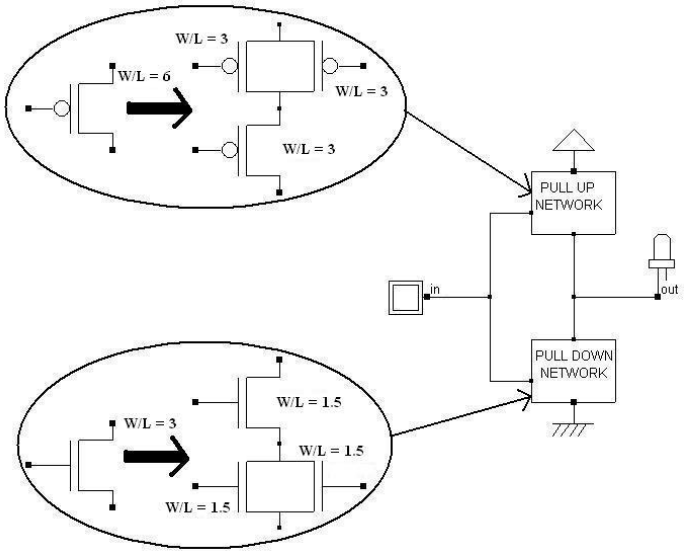

***Figure 6** : Sleepy Stack*

4 EXPERIMENTAL METHODOLOGY

For experimental investigation of all CMOS inverter techniques, two types of software tools are used. Figure 7 shows experimental methodology. For schematic purpose DSCH has been used and for layout designs MICROWIND has been used. Schematic circuit and layouts are design for all type of CMOS inverter approaches. Schematic are used for to make a different type of digital and analogue circuit and all the parameter are estimated with the help of MICROWIND window where the layout are design. These parameter are power dissipation and layout area at different technology of all considering approach. Schematics are designed for all considered techniques using schematics editor i.e. DSCH Window in MICOWIND software tool targeting TSMC are used to obtain net lists of the circuits and the net lists are used to simulating purpose. Inverter based on conventional CMOS, forced NMOS, forced PMOS, forced 2NMOS, stack approach and sleepy stack approach are designed and simulation results have been taken in terms of power dissipation and layout area.

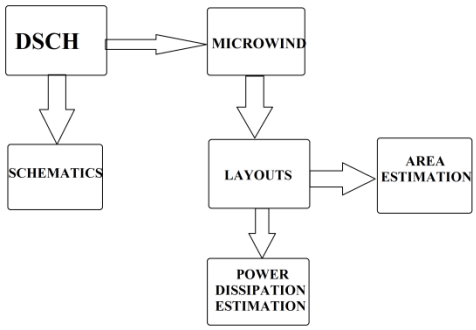

***Figure 7** - Experimental Methodology*

5 SIMULATION RESULTS

Schematic circuits of inverter using different techniques have been designed in DSCH. Different supply voltages have been considered at different technologies. Table 1 shows the value of supply voltages at different technologies.

Table 1 :supply voltages at different technologies

Technology	45 nm	65 nm	90 nm	120 nm
Vdd	0.4 v	0.7 v	1.2 v	1.2 v

Simulation results have been carried out for all techniques at different technologies from 45 nm to 120 nm. Table 2 shows power dissipation in all techniques at different technologies. As the technology scales down, power dissipation in all techniques reduces because of applied supply voltage. From the table 2, it is observed that power dissipation in sleepy stack technique is minimum as compared to all techniques. In 45 nm technology, power dissipation in sleepy stack technique is 0.045 µw, which is 47.6% less as compared to conventional CMOS technique.

Table 2 : Power dissipation using different techniques

Techniques	45 nm (µw)	65 nm (µw)	90 nm (µw)	120 nm (µw)
Conventional CMOS	0.086	0.373	1.546	2.859
Forced NMOS transistor	0.075	0.333	1.251	2.451
Forced NMOS transistor	0.069	0.301	1.199	2.425
Forced 2 NMOS transistor	0.055	0.249	1.099	2.190
Stack	0.051	0.199	0.958	1.510
Sleepy stack	0.045	0.189	0.664	1.000

Other than power dissipation, layout area of circuit is also very important parameter to examine the technique in VLSI design. Layout of inverter using different techniques also examined using MICROWIND tool at different technologies from 45 nm to 120 nm. Table 3 shows the comparative analysis of layout area of inverter using different technique at different technologies. From the observation table, it has been observed that area consumption is more in sleepy stack technique as compared to conventional CMOS technique because numbers of transistors in sleepy stack are more.

Table 3 : Layout area using different techniques

Techniques	45 nm (μm^2)	65 nm (μm^2)	90 nm (μm^2)	120 nm (μm^2)
Conventional CMOS	6.1	12.0	13.9	27.2
Forced NMOS transistor	9.4	18.3	20.7	37.8
Forced NMOS transistor	8.6	16.8	18.9	45.7
Forced 2 NMOS transistor	13.0	25.5	28.5	49.7
Stack	12.0	23.5	26.2	53.7
Sleepy stack	21.7	23.5	47.0	97.7

6 CONCLUSION

In this paper, comparative analysis of inverter circuit has been done using standard CMOS technique to sleepy stack technique. Other inverter techniques are forced NMOS, forced PMOS, forced 2 NMOS and stack approach are also analyzed. Schematic circuit design and Layout design of inverter using all techniques have been done in DSCH and MICROWIND tool. Power dissipation and area consumption have been calculated for all techniques. It is concluded that power dissipation in sleepy stack approach is very less as compared to other techniques but the area increases due to more number of transistor count. Power dissipation in sleepy stack approach is 47.6% less as compared to conventional CMOS technique in 45 nm technology.

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