Exploration Of N-Finfet On Various Gate Materials In 22nm And 20nm Technology

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Abstract: A FinFET device is used to overcome the lithography and performance gain challenges. This paper investigates the transfer characteristics of double gate n- FinFET on different gate materials. Here a double gate n- FinFET with a gate length of both 22 nm and 20 nm has been reported. The on-current (Ion), off-current (Ioff), threshold voltage (Vt) and transconductance (gm) varies on different gate materials. In addition, a FinFET device with high k- dielectric material called hafnium oxide is used in order to increase the drain current and also exhibit the better performance of the device. From the reported work we obtain the following Ion/Ioff ratio as $1.924x10^4$, $1.47x10^{10}$ and $3.11x10^{11}$ for aluminum, molybdenum and Gold gate materials respectively at 22 nm technology. For 20 nm technology, we obtain the Ion/Ioff ratio of molybdenum and gold gate material as $1.73x10^5$ and $0.53x10^3$ respectively. The low threshold voltage was obtain as 0.393V when we used the aluminum as gate material at 22 nm technology and also we got 0.33V as threshold voltage when the molybdenum was used as gate material at 20 nm technology. All the simulations have been done in TCAD which refers to the use of computer simulation to develop and optimize semiconductor processing technologies and devices.

Index Terms: Field Effect Transistor (FinFET), TCAD, Double gate MOSFET, multi-gate field-effect transistors (MuGFET), transconductance, threshold voltage, multi-gate transistor, high-k dielectric

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1. INTRODUCTION

THIS The amount of transistors in an integrated circuit doubles every two years, according to Moore's law. Several strategies to scale down the size of CMOS technology have been developed [1-3]. The multi-gate transistor is one such approach. MOSFET is referred to as a multi-gate transistor with more than one gate in a single device. FinFET is a multi-gate form and a transistor that is non-planar. It has front and back gates that provide better control for the impact of the short channel. Double gate devices are therefore best suited for low-power systems as they allow significant reduction in standby power together with enhanced efficiency. FinFET is characterized by the wrapping of the conducting channel around a thin silicon film that forms the device's body. The fin size determines the device's efficient channel length and gate width. Due to the drift of electron features in the channel and the shift in threshold voltage owing to the shrinking channel length, the brief channel impacts occur. The thin silicon film in the SOI device limits the off-state leakage. The silicon film thickness must be less than one quarter of the length of the channel [4]. For standard bulk MOSFETs, the elevated concentration punch through stopper outcomes in leakage degradation and severe drivability in the gate controls the power barrier between source and drain. Because of the short channel effect [3,22], the self-aligned double gate MOSFET design has a big sub-threshold swing. FinFET is the successful tool that does not compensate for the device's size beyond the limit and efficiency. Using high k dielectric [4, 30-33], the leakage current is decreased. MOSFET double gate is best suited for low-power or high-performance devices in the future. Manufacturing MOSFET double gate devices is more complex than manufacturing single door devices [5-8]. Fig.1. shows the schematic view of FinFET with the geometrical parameter such as gate length (Lg), fin width (Wfin) and fin height (Hfin). It can be inferred that, a metal gate and high k dielectric gives a good performance in nanometer range. In this work, section 2 describes the simulation of n-FinFET in TCAD software with a gate length of 22nm and 20nm technology. Different gate materials like aluminum, molybdenum and gold were used. For each gate metal results have been obtained and the transfer characteristics for each gate metal were then plotted and a comparison was made between them.

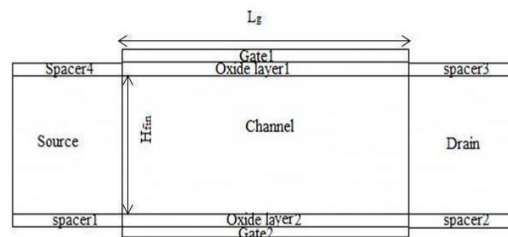

Fig. 1. *Schematic view of FinFET device.*

Manufacturing MOSFET double gate devices is more complex than manufacturing single door devices [9-11]. Fig.1. shows the schematic view of FinFET with the geometrical parameter such as gate length (Lg), fin width (Wfin) and fin height (Hfin). It can be inferred that, a metal gate and high k dielectric gives a good performance in nanometer range [12, 25-26]. In this work, section 2 describes the simulation of n-FinFET in TCAD software with a gate length of 22nm and 20nm technology. Different gate materials like aluminum, molybdenum and gold were used. For each gate metal results have been obtained and the transfer characteristics for each gate metal were then

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plotted and a comparison was made between them. The key feature in a FinFET is the formation of ultra-thin Silicon (Si) fins which forms the transistor channel to reduce the short channel effects. A FinFET can have multiple fins [27-29] as per the process design. Multiple fins are usually used to achieve larger channel width. The dimension of this non-planar device affects the performance in terms of power dissipation and delay.

Effective channel length Leff = Lgate + 2×Lext (1)
Effective channel width W = Tfin + 2×Hfin (2)

Where Hfin and Tfin the fin height and thickness respectively, Lgate is length of the gate, Lext is extended source or drain region as explained in Figure 1. Fin width (Tfin) plays a major role for controlling the short channel effect effectively. Therefore Tfin ~ Lgate/2 is followed. The gate control over the channel was enhanced by integrating multi-gate equipment or multiple gate field-effect transistors (MuGFET) to tackle these problems. The Double Gate Metal Oxide Semiconductor Field Effect Transistor (DGMOSFET) provides better control of brief channel impacts, lowers leakage currents, and increases CMOS scaling efficiency [22]. The fin-type field-effect transistors (FinFETs) are among those the most promising device design to solve these problems and are most compatible with standard CMOS. This makes it simpler to display the manufacturing procedures in Table 1.

TABLE 1
COMPARISON OF MOSFET AND FINFET

MOSFET	FinFET
The main obstacle is that the control of current leakage is difficult.	The presence of multiple fins helps reduce leakage currents.
It is difficult to obtain higher on currents in bulk MOSFET.	It is easier to obtain higher on currents using multiple fins.
Power Dissipation is more.	Power Dissipation is less.
It is a planar device as the current flows parallel to wafer and the channel is placed on wafer plane.	It is a quasi-planar device - as the current flows parallel to wafer and the channel is perpendicular to wafer plane.
Only one gate is present to control the channel.	Two gates are present to control the channel hence reducing short channel effect. This is available in Short Gate (SG) and Independent Gate (IG) mode.
I_{off} -the drain current when V_{gs}=0, V_{ds}=V_{dd} (Ideally 0) increases as it goes further away from the gate.	Due to double gate, the gate capacitance is doubled, hence limiting I_{off} (Ideally 0).

2. 2D N-FINFET DEVICE CREATION

An ultra-thin Si fin in a FinFET framework forms a conducting channel in which the electrons flow from source to drain. This conducting channel is enclosed by a gate that supplies the input voltages. Therefore, controlling electrons flow even in off-state prevents current leakage. There is often an increase in the quantity of charging carriers and the speed at which they flow, leading in the breakdown of the single-fin conducting channel. This blocks the current flow of electrons from source to drain. In multi-gate field-effect transistors (MuGFET), which are built parallel to each other, the number of fins is increased, improving the short channel effect. The amount of charging carriers flowing from greater potential to reduced potential is also increasing as the number of fins rises. The rate at which the carriers flow furthermore increases the switching speed more rapidly. Better gate control over the conducting channel is the primary benefit of various fins. Because of this, the current leakage and the dissipation of energy are reduced. This attains high on-state drive current. The modeling of 2D n-FinFET has been done in TCAD. FinFET device consist of source, drain, double gate, oxide layer and four nitride spacers. Here N-type FinFET was created at both 22nm and 20nm technology. The source and drain was doped with N-type material like Phosphorous [16-18]. The Channel was doped with P-type material like Boron. The doping concentration of source/drain and channel is 1e+18 and 1e+20. The silicon material is used for source, drain and channel region. Four spacers are used in order to improve the ON current [14-15]. The spacers were made up of nitride material Dual material spacers and triple material spacers can also be brought into use for further improvement in device performance. The work function of both front and back gate varies based on different gate material. In order to improve the drain current, the high k dielectric material called hafnium oxide was used in the oxide layer. The height of the FinFET is 10nm. The different parameters of this structure are assumed as follows in the Table 2. The two dimensional schematic view of double gate n-FinFET in TCAD software is as shown in the Fig.2.

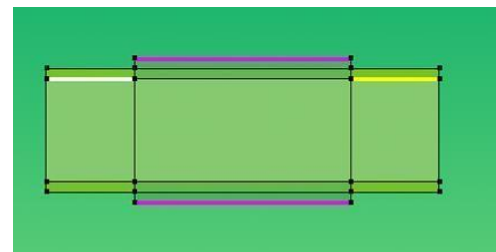

Fig. 2. *2D view of the n-FinFET double gate in TCAD software.*

Parameters	Dimensions
Length of Gate (L_g)	22 nm/20 nm
Spacer Width	1 nm
Gate oxide thickness	1 nm
Height of Fin	10 nm
Doping concentration of source to drain	1e+18
Doping concentration of channel	1e+20

To modulate its electrical characteristics, doping is deliberately introduces impurities into an incredibly pure intrinsic semiconductor. The impurities depend on the type of semiconductor and the characteristics for its desired function that it wants to have. Semiconductors that are lightly and moderately doped are called extrinsic semiconductors. A semiconductor doped to such elevated concentrations is referred to as a degenerative semiconductor that it acts more like a conductor than a semiconductor. The doping profile in n-FinFET in TCAD is shown in Fig.

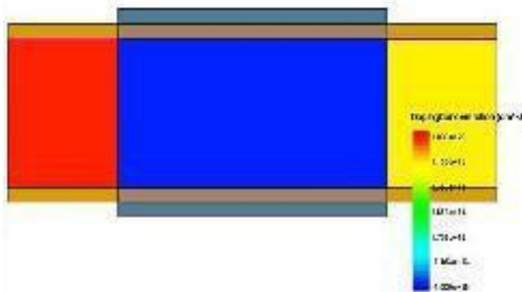

***Fig. 3**. Net doping profile of n-FinFET in TCAD Software*

Doping is performed according to the type of device needed, mesh is the next step. Meshing is performed to get mesh points including all discrete points that are called nodes or vertices. FinFET is a double-gate MOSFET, however to keep the short channel effect in MOSFET in control, the number of gates are increased forming multi-gate field effect transistor (MuGFET). MuGFET devices with the conduction channels wrapped around Si fins are considered to one of the most promising device for enabling further complementary metal oxide semiconductor [21]. This allows better drive current and channel control. Among all multi-gate field effect transistors, the FinFET is widely accepted device.

3 SIMULATION AND RESULTS

TCAD traced the 2D n-FinFET structure and the meshing was effectively completed. Different materials from those in the gate were used. The characteristic of the transition varies depending on different gate materials and a set of outcomes was acquired and the comparison between them was made. The gate voltage was maintained constant for Id / Vg features and the drain voltage should vary. The drain voltage was held constant for Id / Vd characteristics and the voltage of the gate should vary. The Inspect instrument is used to analyze doping profiles and semiconductor device electrical features. The current is obtained when the charge flows from source to drain when the device's on-current (Ion) is applied to the gate voltage (Vg). When Vg is higher than threshold voltage (Vt), the transistor is on. Threshold voltage is a minimum voltage needed to generate a route between the source and the drain. For various gate metals, threshold voltage and transconductance were discovered here on current, off present. For n-FinFET at 22 nm gate length for different gate materials, the transfer characteristics were first discovered and then the gate length is scaled down to 20 nm. Secondly, the transfer characteristics for n-FinFET for various gate materials were found at 20 nm. The values were finally tabulated and the comparison between them was created. If the length of the gate is further lowered, the current of the leakage will increase. The Fig.4. Shows the plot of Id/Vg curve of n-FinFET (Aluminum as gate metal) for Vd=0.6V and Vg=1V. When aluminum was used as gate material, the work function will be 4.17 eV. From the graph we can calculate the on-current and off-current by selecting the curve data from the tool bar.

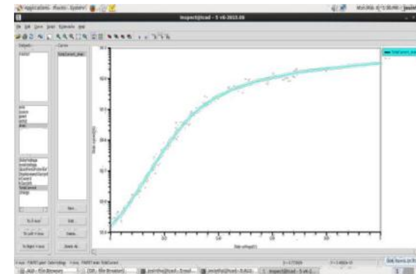

***Fig. 4.** Id/Vg curve of n-FinFET (Aluminum as gate metal) at 22 nm*

The on-current and off-current is low when the aluminum was used as a gate metal. When the Ion/Ioff ratio is low then the device performance will also be low. So secondly we changed the gate metal to molybdenum which has a work function of 4.6eV to achieve higher performance. The Fig.5. Shows the Id/Vg curve of n-FinFET (Molybdenum as gate material) for Vd=0.6V and Vg=1V.

TABLE 4

COMPARISON OF N-FINFET FOR DIFFERENT GATE METAL FOR VG=1V AND VD=0.6V AT 22 NM TECHNOLOGY

Gate Material	I_{ON}	I_{OFF}	Vt (V)	g_m (mho)
Molybdenum	3.30×10^{-4}	1.90×10^{-9}	0.33	0.00055
Gold	2.42×10^{-8}	4.56×10^{-11}	0.93	7.8×10^{-7}

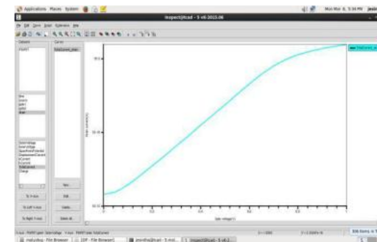

***Fig. 5.** Id/Vg curve of n-FinFET (Molybdenum as gate metal) at 22 nm*

When molybdenum is used as gate metal the ON current and OFF current is little bit greater than ON and OFF current achieved before. In order to further improvement we have changed the gate metal to gold which has a greater work function of 5.2eV. Fig. 6 shows the Id/Vg curve of n-FinFET (Gold as gate material) for Vd=0.6V and Vg=1V.

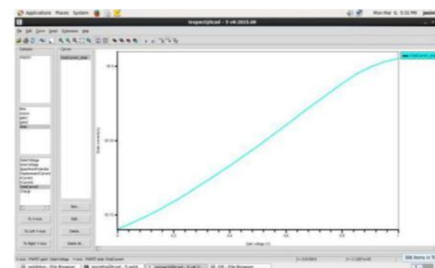

***Fig. 6.** Id/Vg curve of n-FinFET (Gold as gate metal) at 22*

After finding out the characteristics of n-FinFET at 22nm technology we have further reduced the gate length in order to find the transfer characteristics at 20nm technology and there we have used two different gate materials such as gold and molybdenum. Fig. 7and Fig. 8 shows the ID/Vg curve of n-Finfet at 20nm technology of gate materials molybdenum and aluminum respectively.

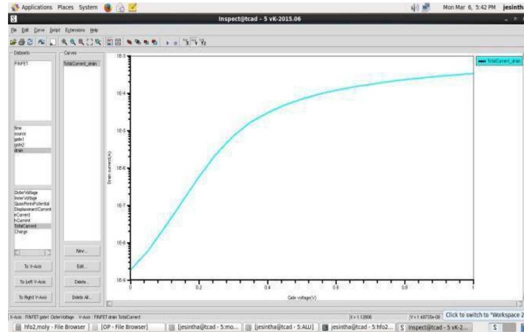

Fig. 7. *Id/Vg curve of n-FinFET (Molybdenum as gate metal) at 20 nm.*

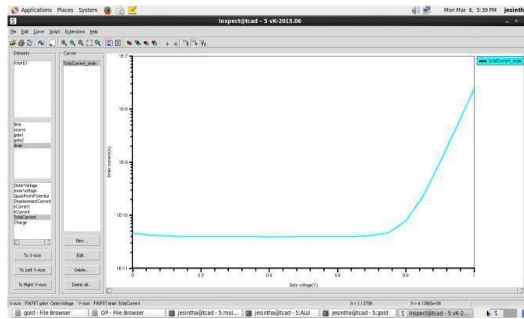

Fig. 8. *Id/Vg curve of n-FinFET (Gold as gate metal) at 20 nm.*

Table 3 and Table 4 shows the comparison of n-FinFET for different gate materials at 22 nm and 20 nm technologies. The obtained on-current (Ion), off-current (Ioff), threshold voltage (Vt) and the transconductane (gm) for various gate materials at both 22nm and 20 nm technology are listed in the table.
The transfer characteristics of the FinFET under different gate materials have been obtained and the comparison between the obtained transfer characteristics has been tabulated. It has been observed that the best transfer characteristics were obtained for that of hafnium as dielectric followed by gate material.

4 CONCLUSION

Double gate based n-FinFET has been designed and simulated at 22 nm and 20 nm technology. In double gate n-FinFET, the various gate metals of Aluminum, Molybdenum and Gold of dielectric thickness 1nm were used. By using the hafnium oxide which has the high k dielectric constant as the gate dielectric we can reduce the leakage current and can improve the performance of the device. From the results it is shown that the combination of Gold gate metal and hafnium oxide has a larger Ion /Ioff ratio than the Aluminum. So it improves the device performance. In future we can use the zirconium oxide as a gate dielectric for further improvement in device performance. Dual nitride spacers can also be used. Dual nitride spacers mean spacer with two different dielectrics. Germanium can be introduced into the channel region in place of silicon for better performance.

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TABLE 3
COMPARISON OF N-FINFET FOR DIFFERENT GATE METAL FOR VG=1V AND VD=0.6V AT 22 NM TECHNOLOGY

Gate Material	I_{ON}	I_{OFF}	Vt (V)	g_m (mho)
Aluminum	3.06×10^{-5}	1.59×10^{-9}	0.393	0.00052
Molybdenum	9.19×10^{-5}	6.23×10^{-15}	0.79	0.00050
Gold	3.46×10^{-5}	1.11×10^{-16}	0.88	0.00040

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