Design Of DAC Using Binary-Controlled Pass-Transistors And A Voltage Summer

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Abstract: In this work, general design architecture for n-bit digital to analog converter (DAC) using binary-controlled analog multiplexers and voltage summer is introduced. Then a circuit level design for 8-bit DAC is portrayed where pass-transistors are configured to act as the binary-controlled analog multiplexers and a conventional op-amp based voltage summer is used. The designed 8-bit DAC is simulated using broadband op-amp and the simulation results indicate that it can work with accepted performance for data rates higher than 1G Symbol/s.

Index Terms: Digital to Analog Converters; Binary-Controlled; Pass-Transistors;

1 INTRODUCTION

The continuous growth of digital electronics applications such as computers and cell phones raises the importance of achieving more designs of ADCs and DACs with higher performance [1-19]. Many DAC designs have been introduced for tens of years. Some DAC designs are based on binary weighted capacitors [1-2]. Some other designs target the compactness [3-4] of the DAC. More other DAC design trends reviewed in [5]. The most common types of DAC have been presented in [20]. These types of DAC are, Pulse-width modulator DAC, Over-sampling DAC, Binary weighted DAC, and R2R ladder DAC. Pulse-width modulator DAC is designed so that the digital input is used to control the switching of a constant signal which could be voltage or current. The resulted signal is then passed through low pass filter in order to produce the corresponding analog output. Over-sampling DAC is classified as interpolation based DAC. In this type of DAC a pulse density conversion approach is employed in order to convert digital bits into analog signal. Due to its low cost and high linearity, this DAC type is preferred when very high resolution is needed, for example more than 16 bits. Binary weighted DAC uses different electrical path for each bit of the digital input to the DAC. The analog output value is obtained as the summation of the voltages or currents that represent the weight of the corresponding input bit. R2R ladder DAC is also considered as binary-weighted DAC. In this type, repetitive cascade assembly of tee resistor R and 2R is used. This arrangement enhances the accuracy since the manufacture of equivalent matched resistors becomes easier. This work uses a configuration that is classified as binary-weighted circuits in order to realize a compact DAC. The concept in this proposed DAC design is the use of NMOS transistors as pass transistors and have them controlled using the binary input of the DAC. The simplicity of pass transistor operation leads to the compactness of the proposed DAC.

2. DETERMINATION OF THE DAC ANALOG OUTPUT

In order to understand how the proposed DAC architecture works, refer to Fig. 1 which explains how a sixteen quantization levels are coded using 4-bits [6-7]. As shown in the figure, the middle level Lm divides the analog output range of the DAC into two equal halves. The analog output of the DAC is greater than the level Lm if the MSB b3 is ‘1’ and less than that level otherwise. In other words, any analog output value higher than Lm must have the MSB of its digital input b3 equals to ‘1’ while any analog output value less than Lm must have b3 equals to ‘0’. So the MSB b3 role is to decide whether the weight of the middle level Lm is added to the analog output or not. Moreover, the other levels that are determined by the remaining three bits are divided by the quantization level Lm into two identical halves with the quantization levels Lq1, and Lq2 divide these two halves into four equal quarters. The difference between the level Lq1 and the level Lm equals to the difference between the level Lq2 and the base level LB and can be both represented by Lq. Consequently, the digital input bit b2 is used to decide whether to add the weight of Lq to the analog output when its value is ‘1’ or not when its value is ‘0’. The same concept applies for all the remaining bits where each binary bit is used to decide whether to add a specific weight to the analog output or not where the weight of each bit is half of the weight of the preceding bit starting from the MSB. This concept can be formulated using Eq. (1):

\[ (V_a) = bN-1 V_m + bN-2 V_m/2 + \ldots +bo V_m/2N-1 \]  

Eq. (1) can be rewritten as:

\[ V_a = \sum_{n=0}^{N-1} b_n \frac{V_m}{2^{n+1}} \]  

Where Va is the analog output, bN-1 is the MSB of the N-bit digital input, Vm is the weight of the quantization level Lm.
3. THE PROPOSED DAC ARCHITECTURE

A general architecture for the proposed DAC is shown in Fig. 2 where each digital bit is used as a selector to an analog multiplexer. The analog multiplexer either produces a zero voltage at its output when the controlling bit is ‘0’ or produces an output voltage that equals to the voltage weight of the controlling bit otherwise. For example, the MSB $b_n$ is used as the selector to the last analog multiplexer in the figure. If $b_n$ is ‘0’ the output of the multiplexer $V_n$ equals to zero (GND) and if $b_n$ is ‘1’ the output of the multiplexer $V_n$ equals the voltage weight of the bit $b_n$ which is $V_m$. The outputs of all the analog multiplexers ($V_0, V_1, \ldots, V_n$) are then summed up by a voltage summer in order to produce the analog output $V_a$ as shown in the figure.

**Fig. 1** The relation between the quantization levels and their codes

**Fig. 2** The proposed DAC architecture
4. THE PROPOSED DAC CIRCUIT REALIZATION

The circuit realization of an 8-bit DAC is shown in Fig. 3 where each block at the DAC architecture shown in Fig. 2 is replaced by one possible circuit realization for that block. The analog voltage multiplexers used at the input stage of the DAC are implemented using pass transistors. Each analog voltage multiplexer is constructed from one PMOS transistor and one NMOS transistor connected as shown in the figure. For example, when the controlling digital bit b7 is '0' the transistor M1 is off while the transistor M2 is on allowing the voltage V7 to be connected to ground through M2. On the other hand, when b7 is '1' the transistor M2 is off while the transistor M1 is on allowing the voltage V7 to be connected to Vm through M1.

The voltage outputs of all the analog voltage multiplexers are then summed up using the conventional voltage summer shown in the figure so that the output Va can be expressed as:

$$Va = -(V0 + V1 + V2 + V3 + V4 + V5 + V6 + V7)$$  \hspace{1cm} (3)

Then, by taking the effect of the analog voltage multiplexers the output Va is represented as follows:

$$Va = - \Sigma_{n=0}^{7} b_n \frac{Vm}{2^{7-n}}$$  \hspace{1cm} (4)

**Fig. 3** The proposed 8-bit DAC circuit realization
5. SIMULATION RESULTS
The DAC shown in Fig. 3 is simulated at different symbol rates using broadband op-amp where the digital input starts at "00000000" and count up to reach "11111111" then the sequence is repeated several times. The simulation results at 200MS/s are shown in Fig. 4 where good linearity at the DAC output is noticed. At 1GS/s the DAC still have acceptable linearity as shown in Fig. 5. However, when the DAC is simulated at 2GS/s, its linearity is degraded slightly.

6. CONCLUSION
This work introduces novel n-bit DAC design architecture. A circuit realization for 8-bit DAC based on this novel DAC design architecture is also portrayed. The simulation results indicate that this DAC design can work at high data rates.

Fig. 4 Simulation results of the proposed 8-bit DAC at data rate 200MS/s

Fig. 5 Simulation results of the proposed 8-bit DAC at data rate 1GS/s

Fig. 6 Simulation results of the proposed 8-bit DAC at data rate 2GS/s

REFERENCES
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